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HIDDEN REGENERATIVE LOOPS IN ELECTRONIC ANALOG COMPUTERS

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SUMMARY—This paper presents a detailed analysis of nerative loops in computing machines. Emphasis is placed the manifestation of this problem in an electronic analog puter wherein the detrimental effects of regenerative loops most often reported. Regenerative loops are shown to arise n, in the physical system being considered, coupling occurs ugh an element capable of storing energy. The regenerative-gain is the deciding factor; an analysis of the effects of ing this loop gain in an attempt to stabilize the computing ess is also presented. Results are verified for a simple lem by an electronic analog computer.

Almost everyone experienced in the use of comput- machines, particularly of the electronic analog variety, amiliar with the effects often produced by regenerative s in the computing process. Recent studies of partial erential equation solution[1] by difference techniques electronic analog computers and the instability result- therefrom have necessitated a review of the causes of nerative loops and a study of their effects. Often appearance of this phenomenon in a computer program sufficient to discourage further consideration of the blem. Their effects are manifested in many ways, ging from complete lack of any outward signs of in- bility to equally complete lack of stability, with the puter behaving like an oscillator or bistable multi- rator. In order to analyze the behavior of regenerative s and to illustrate the means available for salvaging desired result in their presence, the LRC circuit of . 1 will be considered and analyzed in terms of the

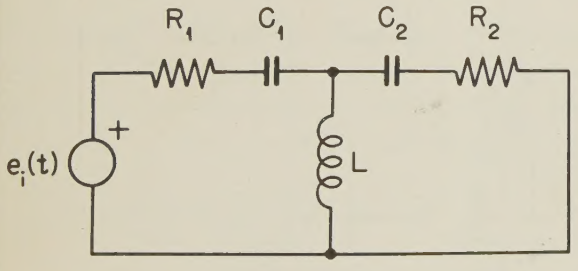


Fig. 1 – LRC circuit with inductive coupling.

nputing machine's short-comings. By summing loop tages around the two independent loops of this circuit, h q_1 and q_2 representing the charges flowing in each p, equations (1a) result:

$$\begin{aligned} \frac{q_1}{c_1} + R_1\dot{q}_1 + L\ddot{q}_1 \qquad & -L\ddot{q}_2 = e_i(t) \\ -L\ddot{q}_1 \qquad & + \frac{q_2}{c_2} + R_2\dot{q}_2 + L\ddot{q}_2 = 0 \end{aligned} \tag{1a}$$

These equations may be expressed in canonical form by defining undamped natural frequencies and damping ratios for each loop as in (2a) below:

$$\begin{aligned} \omega_1^2 q_1 + 2\zeta_1\omega_1\dot{q}_1 + \ddot{q}_1 \qquad & -\ddot{q}_2 = \omega_1^2 q_i \\ -\ddot{q}_1 \qquad & + \omega_2^2 q_2 + 2\zeta_2\omega_2\dot{q}_2 + \ddot{q}_2 = 0 \end{aligned} \tag{2a}$$

$$\omega_k^2 \triangleq \frac{1}{LC_k} \qquad 2\zeta_k\omega_k = \frac{R_k}{L}$$

In similar fashion, the summation of currents at the three independent node pairs of this circuit results in equations (1b), where v_1, v_2, and v_3 are the three independent node voltages:

$$\begin{aligned} & \frac{v_1 - e_i}{R_1} + C_1\frac{d}{dt}(v_1 - v_2) = 0 \\ & C_1\frac{d}{dt}(v_2 - v_1) + C_2\frac{d}{dt}(v_2 - v_3) + \frac{1}{L}\int_0^t v_2\,dt = 0 \\ & \frac{v_3}{R_2} + C_2\frac{d}{dt}(v_3 - v_2) = 0 \end{aligned} \tag{1b}$$

By choosing to represent system parameters as before, the three node-pair equations take the form:

$$\begin{aligned} \frac{\omega_1}{2\zeta_1}v_1 + \dot{v}_1 \qquad & -\dot{v}_2 = \frac{\omega_1}{2\zeta_1}e_i \\ -\frac{\omega_1^2}{\omega_1 2 + \omega_2^2}\dot{v}_1 + \dot{v}_2 + \frac{1}{\omega_1^2 + \omega_2^2}\int_0^t v_2\,dt - \frac{\omega_2^2}{\omega_1^2 + \omega_2^2}\dot{v}_3 = 0 \\ -\dot{v}_2 \qquad & + \frac{\omega_2}{2\zeta_2}v_3 + \dot{v}_3 = 0 \end{aligned} \tag{2b}$$

Figs. 2a and 2b represent, respectively, the analog computer programs capable of solving this LRC circuit on the loop and node basis. Note that these configurations give rise to regenerative loops; in the latter case, two regenerative loops are present in which information at the output of a summing amplifier is returned with a sign change at the latter's input. Investigation will disclose that a disturbance at the input of any of the summing amplifiers will be returned to the input via the regenerative loop with the same sign and magnitude. Such a configuration is potentially unstable even though the physical system which the computer simulated may have no energy sources at all.

In judging the ability of a regenerative loop to produce instability, loop gain appears as the important factor. A loop gain of exactly unity, as required in Fig. 2a, for example, is difficult to achieve in an electronic analog computer; a more realistic assessment of the computer's behavior under these circumstances results if the inevitable deviation of the computer's components from perfection is included as a deviation in loop gain from unity, a deviation arbitrarily entered as shown in the latter figure. Under these conditions, the equations which the *computer* is solving, equations (3), may differ slightly from those which the *computing engineer* wishes to solve.

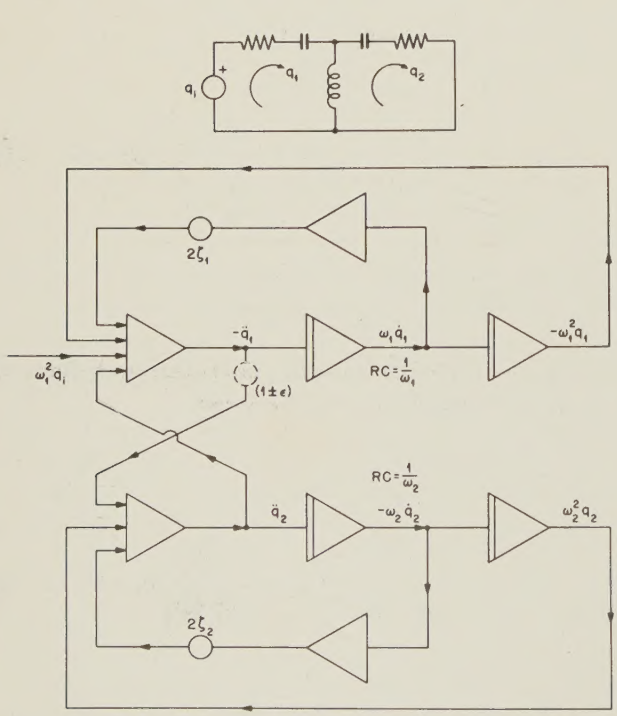
$$\begin{aligned} \ddot{q}_1 &= \ddot{q}_2 + \omega_1^2 q_i \quad - 2\zeta_1\omega_1\dot{q}_1 \quad - \omega_1^2 q_1 \\ \ddot{q}_2 &= (1 \pm \epsilon)\,\ddot{q}_1 \quad - 2\zeta_2 w_2 \dot{q}_2 \quad - \omega_2^2 q_2 \end{aligned} \tag{3}$$

In order to study the behavior of the computer when the regenerative loop gain may deviate from unity, the characteristic equation resulting from equations (3) will be derived. This approach is especially valuable when information relating to the stability of a linear system is desired. Recalling that transients arising in linear invariant equations are always exponential in character, the substitution (exp)st in equations (3) for q_1 after eliminating q_2 results in the characteristic equation of the problem which the computer is, in reality, considering. The most apparent contradiction is the degree of equation (4). A passive linear system with only three energy storing

$$\begin{aligned} \pm\epsilon s^4 + 2(\zeta_2\omega_2 + \zeta_1\omega_1)\, s^3 + (\omega_1^2 + \omega_2^2 + 4\zeta_1\zeta_2\omega_1\omega_2)\, s^2 + \\ + 2\,\omega_1\omega_2\,(\zeta_1\omega_2 + \zeta_2\omega_1)\, s + \omega_1^2\omega_2^2 = 0 \end{aligned} \tag{4}$$

elements cannot define a characteristic equation with more than three roots. The fourth root available in this case must embody the machine's own interpretation of the problem and must be considered as an error term. In the absence of any deviation, the additional root vanishes.

It is most convenient at this point to select typical values for the parameters defined in (2a); these parameters and the corresponding roots of the physical system's characteristic equation are given in (5).



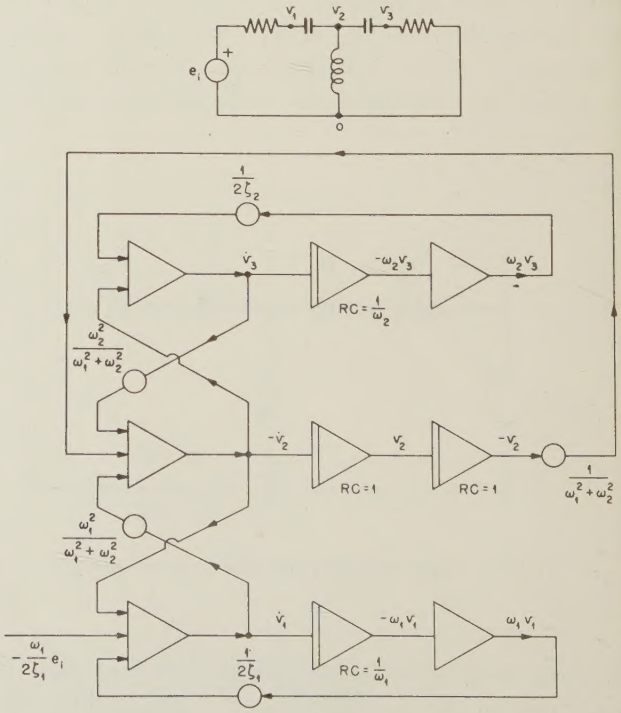


Fig. 2a – Fig. 2b.

or: $\zeta_1 = 0.5 = \zeta_2$

$\omega_1 = 1.0 = \omega_2$

hen (3) becomes:

$$\mp\epsilon s^4 + 2s^3 + 3s^2 + 2s + 1 = 0 \tag{5}$$

or $\epsilon = 0$, the system roots are:

$$s_1 = -1, \; s_2 = -\frac{1}{4} + j\frac{\sqrt{7}}{4}, \; s_3 = -\frac{1}{4} - j\frac{\sqrt{7}}{4}$$

he presence of a very small deviation ϵ, the values of system's roots are scarcely affected and may be ided out of (4), leaving:

$$+1)\left(s + \frac{1}{4} + j\frac{\sqrt{7}}{4}\right)\left(s + \frac{1}{4} - j\frac{\sqrt{7}}{4}\right)\left(\mp\frac{\epsilon}{2}s + 1\right)$$

$$\pm\frac{\epsilon}{2}(3s^3 + 2s^2 + s) = 0 \tag{6}$$

r very small ϵ, the remainder vanishes. The fourth root, wever, becomes alarmingly large and retains the alge- ic sign of the deviation. A loop gain slightly higher n unity will inject into the computing process an un- ble transient term with extremely short time constant l resulting rapid growth. The behavior resulting is not ike that of the flip-flop circuits in common use as mputing devices. A slightly lower loop gain than unity, the other hand, will yield an additional transient term ich decays as rapidly as the former grew and which y not affect the computed result adversely.

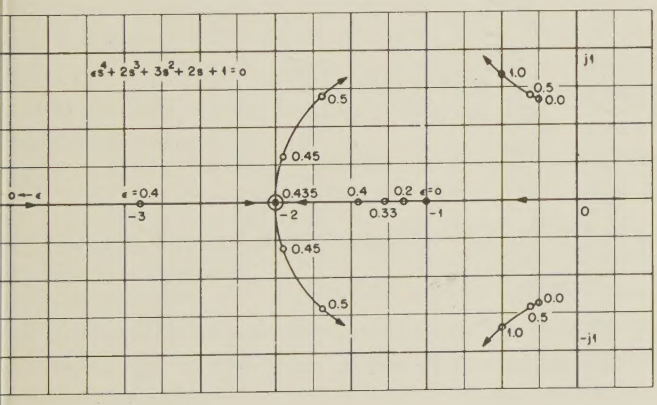


Fig. 3.

The question of just how much loop attenuation is sirable to regain stability is best answered by plotting locus-of-roots chart[2], expressing the position of the aracteristic equations roots as a function of deviation as in Fig. 3. The behavior of the roots for small ϵ is w generalized to larger ϵ, and a large amount of loop enuation is seen to seriously impair the computing ocess by changes in the position of the systems roots and corresponding alteration of the dynamical behavior of the system being considered. These conclusions are illustrated in Fig. 4 by a computer solution of this problem on the loop basis for several negative values of ϵ. Calculation of the amplitudes of the transient terms shows that the amplitude of the unwanted term, in so far as the charge q is concerned, approaches zero as the deviation ϵ becomes small. Insignificant error would result if, in the process of simulating the system, it had not been necessary to generate the higher derivative

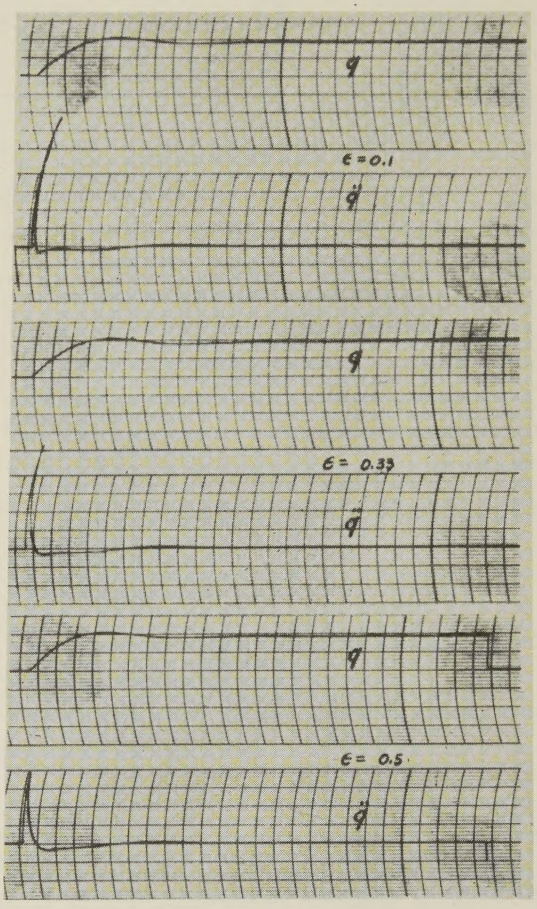


Fig. 4 — Computer solution of equations (3), showing effect of regenerative loop attenuation.

terms of q. The calculated amplitude of the second derivatives become arbitrarily large as the deviation ϵ decreases and is clearly shown in Fig. 4. For a short interval, the summing amplifier generating these derivatives are overloaded and the computing process is interrupted; this is the major source of error resulting from the regenerative loop of unity gain.

This example has demonstrated that difficulty may be encountered when an energy storage element in a system contributes to the *order* of more than one of the simultaneous differential equations describing the system's behavior. The resulting computer program has more integrators than the degree of the system's characteristic equation. A regenerative loop of unity gain is the com-

puter's attempt to cancel the additional roots introduced by these additional integrators; however, cancellation is impossible when the computer's limitations are considered. It is important, then, that an attempt be made to

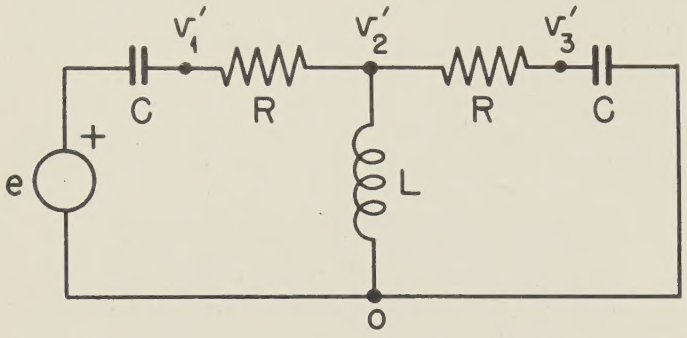


Fig. 5.

arrange the elements comprising the system such that a given energy storage element does not increase the order of more than one of the simultaneous differential equations describing that system. (This statement does not imply that a given element cannot appear in more than one equation.) If the series elements in figure 1 were reversed, as shown in Fig. 5, the node equations (2b) would be modified to the extent shown in equations (7). These are three first order differential equations and,

$$\begin{aligned} T_1\dot{v}_1' + v_1' - v_2' &= T_1\dot{e}_i(t) \\ -v_1' + \frac{1}{T_2}\int v_2\,dt - v_3' &= 0 \\ -v_2' + T_1\dot{v}_3' + v_3' &= 0 \end{aligned} \qquad (7)$$

$$T_1 = RC, \quad T_2 = L/R$$

regardless of the computer's limitations, no more than the three system transients will appear in their solution. The modified computer program, shown in Fig. 6, is free of unity gain regenerative loops and accurately simulates the LRC system's behavior where those shown in Fig. 2 failed.

The results of this analysis may be summarized in a few rules which should help predict the appearance of regenerative loops and help avoid serious problems arising from them. These are as follows:

1. Investigate the physical system, if possible, for coupling through energy storing elements or for the presence of elements which cannot store energy independently of other elements in the system.

2. If such coupling exists, set up the equations for the system on both the loop and node basis. This applies equally well to mechanical[3], electrical and thermal systems. One may lead to a stable computer solution.

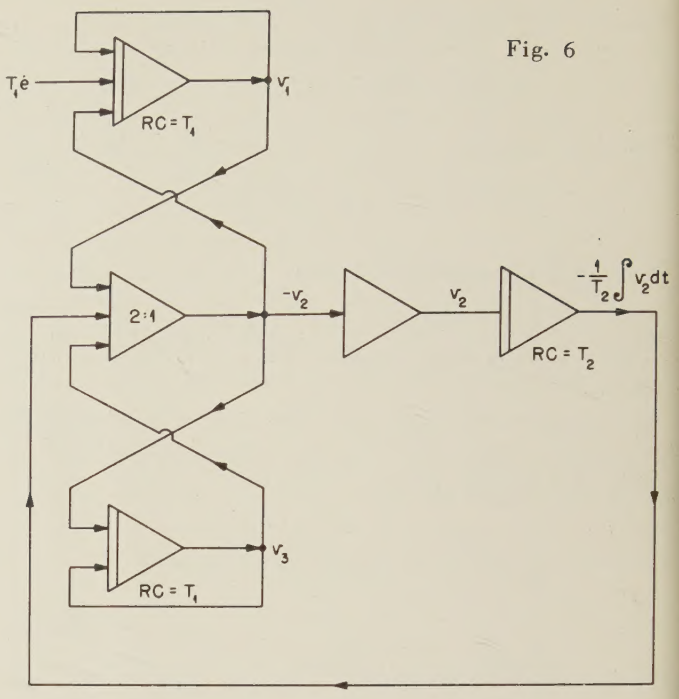


Fig. 6

3. If an energy storing element persists in increasing the order of more than one of the simultaneous equations describing system behavior, investigate the interchange of parallel elements (loop basis) or of series elements (node basis) as a means of obtaining a stable solution.

4. If none of the above suggestions succeed and a unity gain regenerative loop must be employed, introduce a small amount of attentuation in that loop. The amount allowable without threatening the validity of the end result is governed by the shift in the systems roots as well as the magnitude of the transient introduced in the higher derivative terms. These are assessed for the particular problem being studied. Often as much as ten per cent attenuation is allowable.

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3. T. A. Rogers, "Electronic Analog Computers and Partial Differential Equation Solutions," University of California at Los Angeles, Los Angeles, California. (Difference methods for solving partial differential equations by electronic analog computers under some conditions lead to unstable solutions. The author reports this instability in the solution of the one-dimensional wave equation. His techniques are described in the paper.)

ELECTRICAL DELAY LINES FOR DIGITAL COMPUTER APPLICATIONS

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SUMMARY—A survey of existing lumped parameter and tributed parameter delay lines has shown that their maximum age capacity is about 23 pulses and 15 pulses respectively ardless of total delay time. An analysis of pulse transsion through distributed delay lines indicates that dissipa- in the inductive elements is the chief factor limiting age capacity. A method is proposed for decreasing this sipation through the use of high-Q nickel zinc ferrites nd straight conductors for inductive elements.

INTRODUCTION

Electrical delay lines are used in the digital com- er field for storing information, as an adjunct to some ic circuits, for conversion between parallel and serial rations, and to construct word generators.

In addition to their use in civilian and military gital computer projects, they are also being employed experimental high speed telephone switching systems.

While a large selection of electrical properties is ovided by the present types of electrical delay lines ere are still certain disadvantages to these devices. e principal disadvantages are the large volume per it of delay required, high fabrication costs, limited orage capacity, and, in long delay lines, appreciable tenuation. The general trend of reduction in size of mputer and switching systems, particularly with the troduction of transistors into this field, has made it sirable to reduce the size of all other circuit com- nents and networks such as the delay lines. In addi- on, a reduction of attenuation through delay lines ould reduce the total required amplification, thus further creasing the overall size of a computer and perhaps creasing reliability.

This paper presents a brief survey of the perform- ce of commercially available delay lines as storage vice, examines some of the factors limiting delay line rformance, and presents a new construction method for lay lines employing ferrite magnetic materials. This w type of construction appears to offer the advantages er conventional delay lines of reduced volume, lower ansmission loss, lower fabrication cost, and a greater orage capacity.

IMPORTANT CHARACTERISTICS OF DELAY LINES FOR USE IN COMPUTERS OR ELECTRONIC SWITCHING SYSTEMS

The characteristics of delay lines which are important for their application in the computer and switching fields are as follows:

1. Total delay time
2. Rise time of delayed pulse (here defined as the time for the transmitted pulse to rise from 0.1 to 0.9 times its final value)
3. The maximum number of pulses or bits which can be contained in a delay line without interference between adjacent pulses (here defined as total delay divided by twice the rise time)
4. Insertion loss (here defined as the insertion loss for a transmitted pulse rather than the steady state sine wave loss)
5. Volume
6. Pulse distortion due to phase distortion and cross talk
7. Stability of delay with respect to temperature and time
8. Characteristic impedance
9. The ease and accuracy of adjusting delay time to desired values
10. Cost
11. Maximum voltages which can be safely applied across the delay line

The steady state transmission and phase characteristics of delay lines determine the first four characteristics given above. However, in selecting a line for a given purpose it is often very difficult mathematically to translate transmission and phase measurements to rise times, etc., and directly measured data on the latter characteristic are more useful for the computer designer.

A brief study has been made of some available delay lines to determine their characteristics when used as storage devices. The results of this study are presented in Table I. It would be interesting to compare these data with similar data for waveguides and coaxial cables if such data were available. The delay per unit

TABLE I

COMPARISON OF STORAGE CAPACITIES OF ELECTRIC DELAY LINES

Type	Total Delay	Rise Time	Volume, Inches	Z_0 Ohms	Max. Number of Pulses	Pulses Per Cubic Inch	Total Insertion Loss	Insertion Loss per Pulses	Merit Factor*	Min. Pulse Length
LUMPED PARAMETER TYPES										
Commercial Delay Line with 144 Sections and 2 Equalizing T Sections Air Core Coils	4.6 μs	0.1 μs	92.7	430	23	.248	7 db	.304 db	0.816	.2μs
Commercial Delay Line with 100 Sections Ferrite Core Coils	12 μs	0.26	41.2	500	23.1	.56	2	.0866	6.45	.52
Commercial Delay Line with 100 Sections Ferrite Core Coils	200 μs	4.4	74.4	500	22.8	.306	2	.0876	3.5	8.8
DISTRIBUTED PARAMETER TYPES (with spiralled center conductor)										
Commercial 1350 Ohm Distributed Line	4 μs	0.19 μs	–	1350	10.5	–	3.5 db	.333 db	–	.38 μs
	8 μs	0.26	44.6	1350	15.4	.344	8.3	.538	0.64	.52
	12 μs	0.44	77.7	1350	13.6	.175	12.4	.911	0.192	.88
RG 65 U	8 μs	0.31	820	950	12.9	.0157	11.5	.892	0.0176	.62
" "	4 μs	0.18	410	950	11.1	.0271	–	–	–	.36
PROPOSED NEW TYPE OF FERRITE DELAY LINE (Calculated Values Only)										
Lumped parameter ferrite line with Q_L = 200 inductances and 510 mmf miniature mica condensers. 342 Sections	10 μs	.154 μs	40	57	32.4	.81	2.0 db	.062	13	.3μs

*Merit factor = $\frac{\text{Pulses}}{\text{In}^3} \div$ Insertion loss per pulse.

length is of course extremely short in the waveguides and coaxial cables but the corresponding rise times of transmitted pulses are also correspondingly short.

The present limit on storage capacity of lumped parameter delay lines appears to be about 23 pulses or bits regardless of the total delay. The distributed parameter types are limited to a maximum storage capacity of about 15 digits for an optimum length of line (i.e., 8 microseconds for the commercial 1350-ohm type lines). For either shorter or longer lengths than the optimum, the storage capacity becomes less than 15 digits.

For comparison purposes, calculated performance data on a proposed new type of line using ferrite magnetic materials, are also given in Table I. These data show that even without the development of new dielectric or magnetic materials, an improvement in storage capacity and insertion loss and a reduction in volume is possible over the conventional types of delay lines.

SOME FUNDAMENTAL CONSIDERATIONS OF INDUCTIVE AND CAPACITIVE ELEMENTS FOR DELAY LINES

The performance of any delay line, either of the lumped or distributed parameter type, is dependent upon the characteristics of the coils and the condensers or the distributed capacitances and inductances of the line and the geometry of the structure. In order to reduce the volume occupied by delay lines, it would be desirable to use magnetic cores for the coils and fairly high dielectric constant materials in the condensers. In addition, it is quite important that the values of the capacitances and inductances be quite constant over a wide frequency band and that their losses be as low as possible. Data on a number of dielectric and magnetic materials which have been or might be used in constructing delay lines, are presented in table II.

TABLE II

PROPERTIES OF DIELECTRIC AND MAGNETIC MATERIALS WHICH MIGHT BE USED IN ELECTRICAL DELAY LINES

DIELECTRIC MATERIALS

Material	Dielectric Constant K	Frequency Range Over Which K Is Constant*	Material Q			
			60cps	1000cps	1mc	100mc
styrene	2.56	60cps to 25,000mc	> 20,000	> 20,000	14,300	> 10,000
ethylene 3401)	2.56	60cps to 25,000mc	> 5,000	> 5,000	> 5,000	> 5,000
n	2.1	60cps to 25,000mc	> 2,000	> 3,300	> 5,000	> 5,000
Mica	5.4	60cps to 3,000mc	200	1,600	3,300	5,000
ng 790 (SiO_2 Glass)	3.85	60cps to 3,000mc	1,600	1,600	1,600	1,600
ng 707 Glass	4.00	60cps to 3,000mc	1,600	2,000	1,600	830
ium dioxide ure 0-600)	99	60cps to 100mc	1,600	5,000	10,000	1,430
m Titanate 00 Type) **	1500	100cps to 100mc	~130	~120	~100	~40

FERRITE MAGNETIC MATERIALS

Material	Initial Permeability μ_o	Approximate Frequency Range Over Which μ_o Is Constant*°	Material Q At .1mc	Approximate Frequency Range Over which Material Q is Constant*	Frequency at which Q Drops to 10
Zn Ferrite	1500	100cps to 1mc	100	100cps to .01mc	.75mc
roxcube IV C	90	100cps to 32mc	100	100cps to 1mc	16mc
roxcube IV D	45	100cps to 60mc	167	100cps to 8mc	29mc
roxcube IV E	17	100cps to 100mc	167	100cps to 16mc	60mc
ramic E y 174	~750	100cps to 2.5 mc	52	100cps to .2mc	1.2mc

hysical characteristics vary with temperature and applied voltage. Difficult to make to close capacitance tolerances.

ower frequency given is the lowest frequency for which data are available.

The material Q's for the dielectric materials of Table II are defined by:

$$Q_c = \frac{\omega C}{G} = \frac{1}{\tan \delta_c} \tag{1}$$

where G is a shunt conductance across an ideal condenser of capacitance C which uses the given material as a dielectric.
$\tan \delta_c$ is the dissipation factor, and δ_c is the loss angle.

It is assumed in the following discussion that the condensers or distributed capacitances used in delay lines will have negligible resistance and inductance in their leads and plates so that they will approach the idealized condenser of equation (1), in which case they can be represented by a pure capacitance shunted by a conductance. From Table II it can be seen that most of the low dielectric constant materials provide Q's of 1600 or higher and dielectric constants that can be considered constant over a wide frequency range.

Barium titanate with its very high dielectric constant offers the possibility of very small condensers compared to other types. Condensers of this type which are presently available are still far too unstable and have Q values that are too low for use in delay lines. However, the use of barium titanate should not be ruled out for further investigation as a large amount of effort is being expended by various companies in developing materials with lower losses and greater stability.

The smallest commercial condensers using a good dielectric are the button mica type which can be placed in a rectangular volume of 0.0187 cubic inches and the miniature molded mica type which can be placed in a rectangular volume of 0.0293 cubic inches. Both of these types are made in capacitances ranging up to 510 mmf. It is possible to place 34 of the molded mica or 53 of the button mica condensers in each cubic inch of volume.

The condensers used in lumped parameter delay lines all have one side grounded and are all of the same capacitance value. Therefore, it appears that some reduction in volume might be obtained by packaging a large number of condensers with a common ground in a single unit for delay line use. This type of construction would also eliminate one half of the soldered joints now required in making the line.

Only ferrite magnetic materials have been considered for delay lines as these are the only materials available which have constant permeabilities and low losses at frequencies above 1 megacycle. From the data of Table II, it can be seen that the permeability and Q of some of the ferrites are constant over quite a wide frequency range, but the Q's are lower than those of dielectric materials by factors of 10 to 100. The Q of the magnetic material is here defined by:

$$Q_L = \frac{\omega L}{R} = \frac{1}{\tan \delta_L} \tag{2}$$

where L is the inductance of an ideal toroidal coil wound on a toroid of the magnetic material, R is the effective series resistance of the coil due to losses in the magnetic material, and δ_L is the loss angle.

In addition to the material losses in a practical inductance coil, there will also be losses due to eddy currents and proximity effects in the winding and the effective inductance will decrease at high frequencies because of the shunt capacitances of the winding.

THEORETICAL LIMITS IMPOSED ON DELAY LINE STORAGE PERFORMANCE BY DISSIPATION

If there were no losses in capacitive or inductive elements it would be possible to construct lumped parameter type delay lines of any desired storage capacity. It would be necessary only to design individual sections with the proper transmission and phase characteristics (based on low-pass filter design) to give the desired rise time and then add as many sections as necessary to make up the total delay. However, this ideal situation is never met in practice and as has been shown there appears to be an upper limit to the storage capacity of present types of delay lines. Therefore a study has been made to determine the manner in which losses affect rise time for a given total delay assuming that the cutoff frequency without dissipation is high enough not to affect the rise time.

Theoretical calculations of steady state phase and transmission characteristics and pulse rise times for lumped parameter delay lines become quite complex when losses in the coils and condensers are taken into consideration. Because of this complexity, to the knowledge of the writer, no real mathematical attack has been made on the problem. Therefore, it seemed more suitable first to investigate the steady state phase and transmission characteristics and the response to step functions in distributed parameter type delay lines.

It is possible to construct what are essentially distributed parameter lines by using a large number of lumped parameter sections. A lumped parameter line approximates a distributed line when the length of each section is less than one-eighth wavelength of the transmitted signal[1]. Thus, a lumped parameter type line with 40 sections per microsecond of delay will approximate a distributed line at all frequencies up to 5 megacycles. Let us now look at the performance which can be obtained with such lines.

Ideally if all parameters could be controlled, it would be desirable to design the classical distortionless transmission line. In such a line, we must satisfy the condition:

$$LG = RC \tag{3}$$

where L is the distributed series inductance per unit length,
C is the distributed shunt capacitance per unit length,
R is the distributed series resistance per unit length, and
G is the distributed shunt conductance per unit length.

The delay time T per unit length will then be:

$$T = \sqrt{LC} \tag{4}$$

The characteristic impedance of the line can be expressed by:

$$Z_o = \sqrt{\frac{L}{C}} \tag{5}$$

and the attenuation constant α per unit length will be:

$$\alpha = \sqrt{GR} = R\sqrt{\frac{C}{L}} \cdot \frac{R}{L}\sqrt{LC} \tag{6}$$

In any practical structure L and C can be made constant over a wide frequency range, but G and R will vary with frequency. Therefore, to approach the distortionless line even over a limited frequency band it is usual to add a large amount of series resistance and shunt conductance that is constant with frequency. This has the disadvantages of greatly increasing the insertion loss of the line and adding more physical elements and volume to the structure. For example, a 42-ohm 10-microsecond delay line constructed with low-loss magnetic (Q_L = 160) and dielectric materials can be made to satisfy equation (3) out to 10 megacycles only if series resistances totaling 2,040 ohms and shunt conductances totaling 12.2 mhos are added to the line. This would result in an impractical insertion loss of 434.25 db.

If G and R for the distributed line are both directly proportional to frequency (Q_L and Q_c constant versus frequency) we can satisfy equation (3) but in this case the transmission line will be distortionless in phase only. If $Q_L = \frac{\omega L}{R}$ and $Q_c = \frac{\omega C}{G}$ equation (3) then reduces to:

$$Q_L = Q_c \tag{7}$$

Equations (3), (4) and (5) are still valid for this transmission line but the attenuation constant becomes:

$$d = \frac{\omega}{Q}\sqrt{LC} \tag{8}$$

where $Q = Q_L = Q_c$

Assuming that Q_L and Q_c in the line will be determined by the Q's of the dielectric and the magnetic materials let us choose a Q of 160 for each material. Then if it is assumed that Q, L, and C are constant over a 10-megacycle bandwidth, a delay line could be built with a linear phase characteristic over this band. A line of this type having a delay of 10 microseconds would have an insertion loss at 1.78 megacycles which is 6 db greater than the O frequency insertion loss. While such a delay line would have far better phase characteristics than any commercially available lumped delay line, the band width is not exceptional. In addition while a magnetic material such as Ferroxcube IV C might provide the Q assumed, there is not a dielectric material available to match this Q. To obtain an insertion loss which is only 6 db down at 10 megacycles would require a Q of 900 for both the dielectric material and magnetic material. Since the band width of this line (as defined by the 6-db down point) is inversely proportional to the delay time, a wider bandwidth could also be obtained by reducing the delay time.

The next type of transmission line to be considered is that in which Q_C, the Q of the distributed capacitance is very much higher than Q_L, the Q of the distributed inductance. As has been shown in Table II, the Q's for available dielectrics are much higher than those for the available magnetic materials. If Q_L is high enough so $\omega L >> R$ and Q_C is high enough so $\omega C >> G$ then we may write for the attenuation constant[1]:

$$\alpha = \frac{1}{2}\left(R\sqrt{\frac{C}{L}} + \sqrt{\frac{L}{C}}\right) = \frac{\omega}{2}\sqrt{LC}\left(\frac{1}{Q_L} + \frac{1}{Q_C}\right) \tag{9}$$

Now if $1/Q_c$ in equation (9) (which is small compared to $1/Q_L$) is neglected we see that the attenuation constant is 1/2 of that for the previous case (equation (8)) in which Q_C is equal to Q_L. Thus it is advantageous not only from the materials standpoint (it would be difficult to obtain equal values for Q_C and Q_L in practice) but also for reducing attenuation to use a dielectric whose loss is as low as possible. For example, with a Q_L of 200 the insertion loss of a 10 microsecond delay line of this type is 6 db down from O frequency at 4.45 megacycles. A Q_L of 450 is required to move the 6-db down point up to 10 megacycles.

The delay time per unit length of this line is also approximately equal to $\sqrt{LC}$ as in the previous case. This

means that the phase shift in a distributed delay line with low losses and constant permeability and dielectric constant versus frequency is linear even beyond the frequency where the insertion loss is 6 db or greater.

The characteristic impedance for such a line is expressed by[1]:

$$Z_o = \sqrt{\frac{L}{C}}\left[1 - \frac{j}{2}\left(\frac{1}{Q_L} - \frac{1}{Q_C}\right)\right] \tag{10}$$

Here again if Q_L and Q_C are large the impedance will approach a pure resistance equal to $\sqrt{\frac{L}{C}}$.

Mr. L. A. MacColl of Bell Laboratories has derived an expression for the output voltage as a function of time and distance along an infinite transmission line of the above type when a voltage step is applied at the input. The parameters L, C, Q_L, and Q_C, of this line must be constant at all frequencies of interest. This condition is never quite met from a practical standpoint as Q_L and Q_C will always decrease at very low and very high frequencies. However, these assumptions appear to be closer to practical transmission lines than the assumption that R and G are constant at all frequencies. The expression for voltage V when an input voltage step V_o is applied as derived by MacColl is:

$$V(x,t) = V_o\left[\frac{1}{2} + \frac{1}{\pi}\arctan\left(\frac{t-\beta_o x}{\alpha_o x}\right)\right] \tag{11}$$

where t is time, x is distance along the transmission line, $\alpha_o\omega$ is the attenuation per unit length, and $\beta_o\omega$ is the phase shift per unit length.

Let us now apply equation (11) to a finite transmission or delay line x unit lengths long and terminated in its characteristic impedance. If Q_L and Q_C are large from equation (9) it follows that we may write:

$$\alpha_o = \frac{\sqrt{LC}}{2}\left(\frac{1}{Q_L} + \frac{1}{Q_C}\right) = \frac{\sqrt{LC}}{2}\,\frac{1}{Q'} \tag{12}$$

where

$$Q' = \frac{Q_L\ Q_c}{Q_L + Q_c}$$

Since from reference 1 the phase shift per unit length is $\omega\sqrt{LC}$ we may write:

$$\beta_o = \sqrt{LC} = \text{delay per unit length} \tag{13}$$

$$\beta_o x = x\sqrt{LC} = \text{total delay} = T. \tag{14}$$

By multiplying equation (12) by x and substituting T for $x\sqrt{LC}$ we may then write:

$$\alpha_o x = \frac{T}{2Q'}. \tag{15}$$

If the values derived above for $\beta_o x$ and $\alpha_o x$ are substituted in equation (11), we can solve for t_1, the time at which the output voltage V rises to 0.1 times its final value of V_o. This gives

$$t_1 = T\left(1 - \frac{3.078}{2Q'}\right). \tag{16}$$

In a similar manner we can find the time t_2 at which the output voltage rises to 0.9 times its final value V_o which is:

$$t_2 = T\left(\frac{3.078}{2Q'} + 1\right) \tag{17}$$

If the rise time of the output pulse be defined by $t_2 - t_1$ then we may write:

$$\text{Rise time} = \frac{3.078\,T}{Q'}. \tag{18}$$

Thus the rise time of a voltage step transmitted through this type of line will be directly proportional to the delay and inversely proportional to the resultant Q of the inductance and capacitance per unit length as determined by the materials and structure of the line. The total number of digits or distinct pulses which the line can store as defined in the first section will be:

$$\frac{Q'}{6.156}. \tag{19}$$

Since the Q of most good dielectric materials is at least 10 times the Q of available magnetic materials, Q' will be approximately equal to Q_L. For a Q_L of 200 and Q_C of 2000, the total number of digits becomes 32.4 regardless of the total delay time. It is probable that the presence of dc resistance and leakage conduction in a transmission line while introducing more insertion loss at all frequencies will also increase the effective band width so that the number of digits which can be stored will be somewhat greater than $\frac{Q'}{6.156}$. These dc losses were omitted in deriving equation (11) because of the mathematical complexity they introduced.

A NEW TYPE OF DELAY LINE CONSTRUCTION

Since the Q's of commercially available condensers re quite high and there appears to be no immediate prospect of reducing the size of condenser employing high materials, it was decided to investigate the possibility of improving the performance of lumped-parameter type lines by improving only the inductive elements.

To reduce winding losses and distributed capacitance to a minimum it is proposed that inductive elements for lumped-parameter delay lines be composed of a straight cylindrical conductor surrounded by magnetic material. The inductance elements would then appear as shown in Fig. 1. These inductances have the advantages of a compact and simple construction requiring no coil winding and have almost negligible conductor losses.

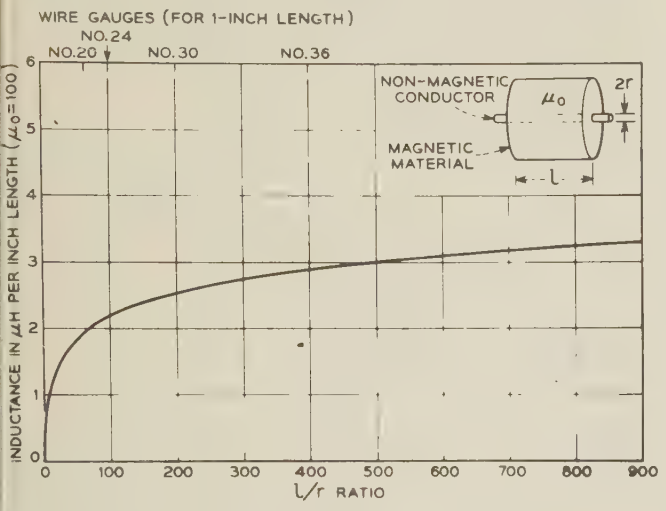

Fig. 1 — Calculated inductance of a finite straight cylindrical conductor in magnetic material.

The Q's of such coils might be increased to twice the material Q's (with a corresponding reduction in inductance) by providing small air gaps. Inductance elements of this type with no air gaps in the magnetic circuit have been measured to have Q's at 2 mc of 186 for the ferroxcube IVD and 156 for the ferroxcube IVC materials.

The inductance of a finite straight nonmagnetic cylindrical conductor is given by[2]:

$$L = 2\mu \left[l \log_e \frac{l + \sqrt{l^2 + r^2}}{r} - \sqrt{l^2 + r^2} + r \right] + \frac{1}{2} \text{ abhenries} \qquad (20)$$

where μ is the relative permeability of the medium surrounding the conductor,
l is the length of the conductor in cm, and
r is the radius of the conductor in cm.

This formula does not take into account any change in inductance with frequency because of skin effects in the conductor. However, where the $\frac{l}{r}$ ratio is large and μ is high and independent of frequency, this effect should be insignificant. If μ is about 50 or higher the last term of equation (20) can be neglected and the inductance formula can be written as

$$L = 0.00508\ \mu l \left[\log_e \left(\frac{l}{r} + \sqrt{\frac{l^2}{r^2} + 1} \right) - \sqrt{l + \frac{r^2}{l^2}} + \frac{r}{l} \right] \text{ microhenries} \qquad (21)$$

where μ is the relative permeability of the medium surrounding the conductor,
l is the conductor length in inches, and
r is the conductor radius in inches.

The inductance versus $\frac{l}{r}$ ratio calculated by equation (21) has been plotted in Fig. 1 for a material with a μ of 100. From this graph it can be seen that very little is to be gained by increasing the $\frac{l}{r}$ ratio beyond 400, which is equivalent to using a one-inch long #36 wire. It is also evident that the maximum practical inductance for a one-inch long wire in a magnetic medium having a μ of 100 is between 2 and 3 microhenries.

The inductance of several MnZn ferrite ($\mu = 1500$) tubes with conductors through the center 3/8 inch long, 3/8 inch O.D., and 0.12 inch I.D., were measured and found to vary from 4.5 to 5.1 microhenries. The value calculated by formula (21) for this size core, by assuming a conductor which just fits the inside diameter of the tube is 4.9 microhenries. From these and other measurements on sample ferrite tubes it appears that the inductance is determined by the inside diameter of the tube and is nearly independent of the diameter of the conductor through the tube.

In summary, it appears feasible to construct coils of the above form which have an inductance of at least 1 microhenry and a Q of about 200 which are both constant to frequencies as high as 8 megacycles. The Q and inductance values given assume that the ferrite tube will contain a small air gap and be about 1 inch long x 1/8 inch outside diameter with an inside diameter of about 0.015 inch. In order to allow close spacing of the inductive elements it is further proposed that they be placed side by side. This will result in some mutual coupling unless air spaces are left between each of the coils. As will be shown below if the mutual coupling is properly chosen it can be used to improve the phase characteristics of the delay line.

It is well known that the phase characteristic of the low-pass filter sections used in lumped-parameter

delay lines can be improved by introducing mutual coupling between adjacent coils. The mutual coupling may be either between alternate coil sections only as shown in Fig. 2a or between every coil section as shown in Fig. 2b. In the former case each T section is equivalent to an m-derived section. Values of m from $\sqrt{1.5}$ to $\sqrt{2}$ which give coupling factors K of 0.2 to 0.33 have been used in various designs. The figure of $\sqrt{1.5}$ for m is obtained when one solves mathematically for a nearly constant time-delay-versus-frequency characteristic by eliminating higher order terms in the expression for delay time in an m-derived low-pass filter section. Values of m greater than $\sqrt{1.5}$ are sometimes used to reduce the amount by which the time delay departs from its average value at frequencies close to cutoff.

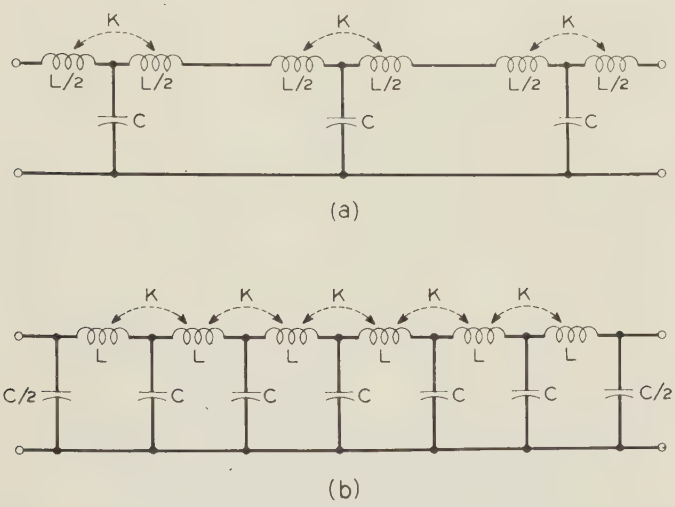

Fig. 2 – (a) Section of a lumped-parameter delay line with coupling K of 0.2 to 0.33 between alternate sections.
(b) Section of a lumped-parameter delay line with coupling K of 0.1 between adjacent sections.

When the coupling is between each adjacent coil section as shown in Fig. 2b, a solution of the equation for delay time to give the most constant time delay versus frequency results in a coupling factor K of 0.1. Thus the coupling in this type of structure can only be one half of that for the structure of Fig. 2a.

In the proposed type of delay line structure employing a single conductor surrounded by ferrite magnetic material, it is desirable to place adjacent sections as close together as possible to reduce the volume. The physical structure of a delay line of the type shown in Fig. 2a is shown in Fig. 3. The coupling between the T sections is nearly eliminated by a large air space between them. The coupling between the two inductive elements of each T section is of course determined by the spacing between the parallel conductors and the length of the conductors. For conductor lengths of 0.7 inch a spacing of about 0.3 inch is required between the conductors to give a coupling factor K of 0.2. The inductive elements are constructed by cutting two slots about 0.01 by 0.01 inch in a block of ferrite and then placing another block of ferrite over the slotted block. Much smaller holes can be obtained in this manner than by molding a complete unit and an air gap is also provided for improving the Q of the inductive elements.[3] If ferroxcube IVC is used for the magnetic material, an inductance of about 0.72 μh can be obtained in a 0.7 inch length with an insulated #33 wire through the 0.01 inch slot.

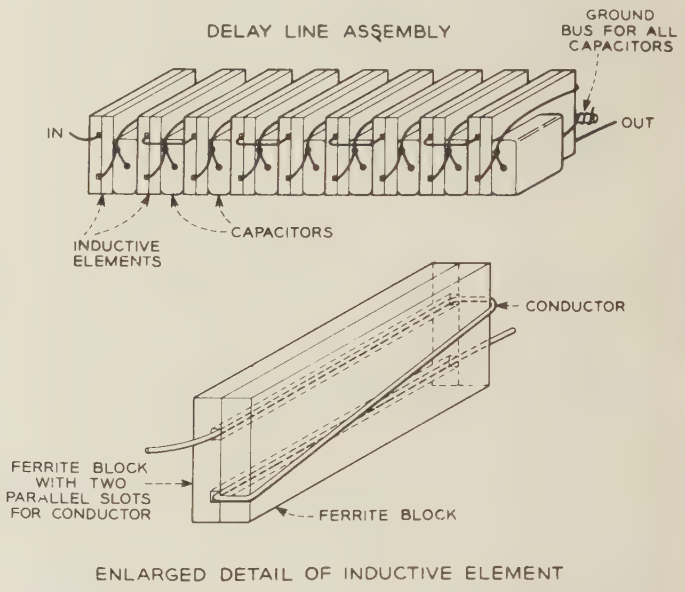

Fig. 3 – Physical construction of ferrite block delay line for circuit of Fig. 2(a).

Two methods of constructing a delay line with coupling between each of the adjacent inductive elements are shown in Fig. 4. The structure at the top of Fig. 4 is fairly simple in that a lot of inductive elements can be constructed from only two blocks of ferrite magnetic material. However, the spacing between conductors must be quite large to obtain a coupling factor K as low as 0.1. An experimental line of this type comprising 18 sections is illustrated in Fig. 5 and its measured phase and insertion loss characteristics are shown in Fig. 6. The conductors of the inductive elements were quite close together giving a coupling coefficient of 0.3. This accounts for the deviation from a linear phase characteristic shown in Fig. 6.

The coupling between sections can be reduced considerably without increasing the over-all volume by having an air space between the upper portion of the ferrite blocks as shown in the lower part of Fig. 4.

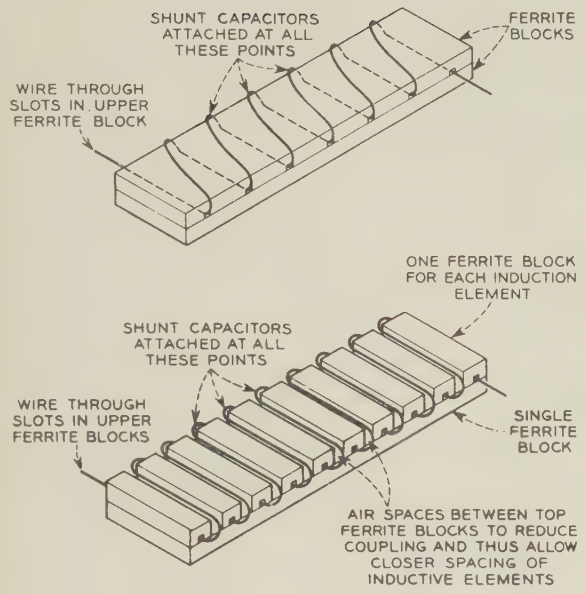

Fig. 4 – Two methods of constructing ferrite block delay lines with coupling between adjacent inductances as shown in the circuit of Fig. 2(b).

CONCLUSIONS

A survey of existing lumped parameter and distributed parameter electrical delay lines has shown that a maximum of 23 pulses and 15 pulses respectively can be stored in these devices irrespective of total delay time. Theoretical analysis of pulse transmission through distributed-parameter lines indicates that dissipation in the inductive elements is the chief factor limiting storage capacity. In order to increase the storage capacity and reduce the volume and insertion loss of these lines, an investigation has been made of using ferrites in special forms for the inductance elements. It appears that the volume and insertion loss can be reduced and storage capacity increased to about 32 pulses by using low permeability high-Q nickel-zinc ferrites around straight single conductors for the inductance elements. In addition, coil windings and many of the soldered joints now used in lumped-parameter lines can be eliminated.

ACKNOWLEDGEMENTS

The writer wishes to acknowledge the contributions of many associates to this investigation of delay lines. Experimental ferrite tubes and information on ferrites were provided by C. D. Owens. Data on the 1350 ohm and RG 65 U delay lines were provided by E. L. Younker and J. W. Johnson and by R. L. Carbrey, respectively. L. A. MacColl derived a formula for describing the response to a step function of a special type of transmission line. W. E. Thacker provided steady-state phase and insertion loss data for the experimental delay line. The experimental delay line was constructed and initially tested by E. F. Lyons.

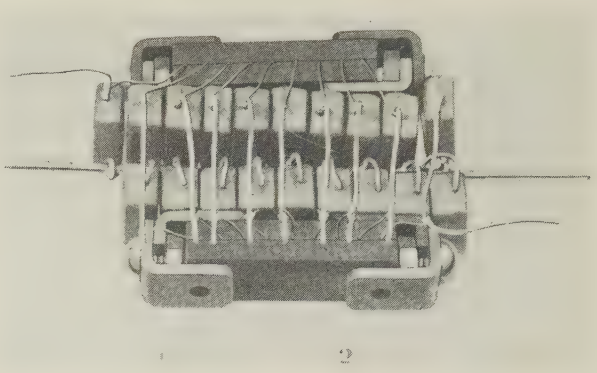

Fig. 5 – Experimental 1/3 μs delay line with ferrite block inductive elements.

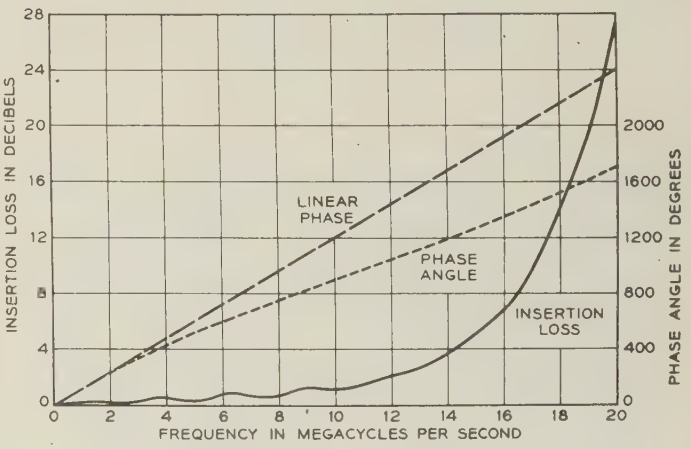

Fig. 6 – Insertion loss and phase versus frequency characteristic for experimental delay line of Fig. 5.

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DESIGN OF TRIODE FLIP-FLOPS FOR LONG-TERM STABILITY

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Summary—Reliable electronic circuit design must account for the parameter variations over the normal life of components to insure satisfactory operation. An analytical design method is derived for an Eccles-Jordan triode flip-flop in which the "worst" condition of voltage and component tolerances conditions are assumed that assures satisfactory operation for normal conditions. The method of analysis is to divide the flip-flop circuit into separate parts, write appropriate equations, and solve them simultaneously. The design method results in the best configurations of component values, regardless of what tube may be used, and actually specifies characteristics which the tube should have, as well as the expected life of the tube in terms of maximum plate resistance.

I. INTRODUCTION

Reliable electronic circuit design must account for the limits of voltage and component variations to insure satisfactory operation. The initial tolerance, plus shelf and load life changes in the value of components, and the drift and regulation of power supply voltages have a major effect on the stability of a circuit. These normal changes in component values and voltages are of particular importance in the design of bistable electronic circuits such as the Eccles-Jordan flip-flop.

An analytical design method is derived for the Eccles-Jordan flip-flop in which signal insertion diodes may be present in the grid circuit and an output divider may be added in the plate circuit. The design method results in the best configuration of component values regardless of the tube type and actually specifies the characteristics the tube should have. This particular approach, as applied to the design of flip-flops, is typical of the basic philosophy of circuit design that is applicable to most electronic circuitry.

The concept of "worst" case is used in which allowances for normal variations of component values and operating voltages can be made, so that unless the component falls outside the broad specified limits satisfactory circuit operation can be obtained. In bistable electronic circuitry the most adverse condition exists when the component tolerance is at one of its extreme limits. In general, each component will assume its opposite extreme limit for each of the two stable states. Therefore, for the purpose of "worst" case circuit analysis the components may be thought of as being bistable devices switching between the two tolerance limits. Any configuration that lies within these computed limits is more favorable than the worst case and will always satisfy the criteria of reliable operation.

The method of analysis is to divide the flip-flop circuit into separate parts, write appropriate equations, and solve them simultaneously. In this presentation, the grid divider is separated from the plate circuit and each is treated for the "worst" case of the two stable states. A common solution of the resulting equations leads to an optimum choice of components as will be described. This approach can be extended to any circuit in which a divider is used to couple the plate of one tube to the grid of another.

The derivation of the analytical solution for the Eccles-Jordan type flip-flop is initially attacked with clamping or insertion diodes in the grid circuit and without an output divider. This results in a set of design equations for a generalized flip-flop.

Three special cases are then treated. The first, the self-biased flip-flop in which a cathode resistor is used; the second, in which the insertion diodes are eliminated and the conventional Eccles-Jordan flip-flop results; and the third, with the insertion diodes in the grid circuit and a tapped output resistor divider in the plate circuit to drive a cathode follower. A typical numerical example of a flip-flop design is presented to illustrate the method.

The emphasis of the present treatment on flip-flop dc stability rather than on switching response arises from the fact that any desired switching response can usually be obtained for a wide range of resistor and tube choices. Because of this wide latitude, efficient use of components suggests an optimum circuit on the basis of dc stability for which a proper choice of transpose capacitors will yield the proper switching response. The following design methods will lead directly to an optimum dc circuit which can then be tested for switching response. Should the switching characteristics dictate a change in the dc design, such a change can be realized in a manner that still ensures as good a dc stability as possible.

II. GENERAL CASE

A. Assumptions

Consider the circuit of Fig. 1. This is the conventional Eccles-Jordan flip-flop to which have been added signal injection diodes. Positive trigger pulses can be injected through D_1; negative trigger pulses through D_2. In addition, these diodes accomplish two purposes: (1) they disconnect the flip-flop grid from the triggering source after the flip-flop has started to trigger; and (2) they prevent excessive excursion of the grid level, thus permitting faster switching and recovery of the cir-

uit. In a circuit designed for dc stability under wide omponent and voltage variations, the transient and uiescent grid voltages are considerably more negative f clamping diodes are not used. As a consequence, if lamping diodes are not used, more time is required for a rid to rise to the conduction level and a longer delay is xperienced in the circuit.

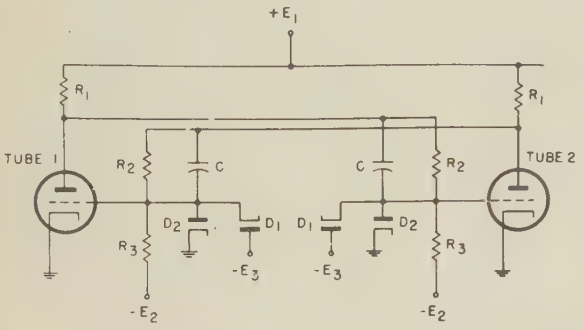

Fig. 1 – Flip-flop with injection diodes.

The transpose (or "speed-up") capacitors enter only into the switching time of the circuit and not its dc stability. Consequently, these capacitors will be disregarded for the remainder of this analysis.

In the design of a flip-flop the input signal is usually dictated by the consideration of associated circuitry. Important factors are the amplitude of signals available from driving sources, limitations of diode circuits, and losses in networks interconnecting flip-flops. For positive input signals, the bias voltage $-E_3$, can be no greater than the available input signal since reliable triggering demands that the grid be moved from $-E_3$ to the cathode level (or, at least, within one or two volts of the cathode.) For negative input signals, the bias voltage need only be chosen to lie below the conduction range according to reliability standards dictated by good engineering practice. It is assumed that the bias voltage is sufficient to make the leakage plate current negative. If no considerations such as these prevail, some value of bias voltage is assumed for initial investigation.

As the tube in the circuit ages, i.e., as the plate resistance increases, the flip-flop approaches the minimum limit of reliability. The maximum plate resistance that can be tolerated will be shown to be independent of specific tube characteristics. However, tube characteristics are pertinent in that they serve to determine the life that can be expected in the circuit from a particular tube. Under certain conditions to be discussed, the maximum plate voltage that can be held cut off by the bias level, $-E_3$, imposes a limiting condition on the design.

Two additional initial specifications are the dc input impedance and the output voltage swing. Attention is focused on the dc input impedance because of its importance in digital computer applications, where crystal diode circuits are used to drive flip-flops. A high dc input impedance is always desirable but in many applications a minimum input impedance is generally imposed by limitations of the driving circuit. Similarly, a large output voltage swing is always desirable, but a minimum voltage swing is generally imposed by the circuits to be driven.

From the above, the following requirements may be imposed on the circuit: (1) a bias level, $-E_3$; (2) a minimum input impedance; and (3) a minimum output voltage swing. It will be shown that the last two are not independent.

First, an analytical expression for the grid divider for the "ON" and "OFF" states will be obtained. Second, an analytical expression for the plate circuit, including the vacuum tube, for the "ON" and "OFF" states will be obtained. Third, a solution that satisfies these two equations will yield the values of all the resistors in the flip-flop circuit.

B. Grid Divider

Attention is initially focused on the grid divider. In Fig. 2 the plate voltage of tube 1 may have two values: a high value, E_{nc}, when tube 1 is nonconducting, or a low value, E_c, when tube 1 is conducting.

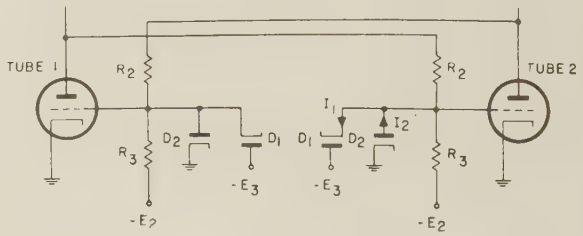

Fig. 2 – Grid circuit.

When tube 1 is nonconducting, the grid voltage of tube 2 should be at least as positive as the cathode voltage. As a consequence, current will flow through R_2 into the back resistance of diode D_1. The "worst" combination of voltage and component tolerances for the grid divider is that condition that tends to depress the grid voltage of tube 2 to its lowest level. This implies that (1) the grid divider resistor R_2 is maximum while R_3 is minimum; (2) the negative bias voltage, $-E_3$, as well as the negative grid divider return voltage, $-E_2$, are most negative; (3) the plate voltage of tube 1, E_{nc}, is at its nonconducting value; and (4) the back resistance of the diode, D_1, is the minimum design value, R_b. Designating minimum values by sub-bars and maximum values by super-bars, the preceding considerations lead to equation (1). The conducting grid voltage of tube 2, G_{c2}, is

$$G_{c2} = O = -\overline{E_2} + \overline{R_3}\left[\frac{E_{nc}}{\overline{R_2}} - I_1\right]$$

where $$I_1 = \frac{\overline{E_3}}{R_b}.$$

If ρ is the permitted fractional resistance tolerance while σ is the permitted fractional voltage tolerance, this relation becomes

$$G_{c2} = O = -(1+\sigma)E_2 + (1-\rho)R_3\left[\frac{E_{nc}}{(1+\rho)R_2} - I_1\right]$$

where $$I_1 = \frac{(1+\sigma)E_3}{R_b}. \qquad (1)$$

When tube 1 is conducting, the grid voltage of tube 2 should be at least as negative as the bias level, $-E_3$. Current will flow *from* the back resistance of diode D_2 into R_3. The "worst" combination of voltage and component tolerances now is that which will tend to raise the grid voltage of tube 2 to its highest level. This implies that (1) the grid divider resistor, R_2, is minimum while R_3 is maximum; (2) the negative bias voltage, $-E_3$, is most negative while the negative grid divider return voltage, $-E_2$, is most positive; (3) the plate voltage of tube 1, E_c, is at its conducting value; and (4) the back resistance of diode, D_2, is the minimum design value, R_b. These conditions lead to equation (2). The nonconducting grid voltage of tube 2, G_{nc2}, is

$$G_{nc2} = -\overline{E}_3 = -\underline{E_2} + \overline{R_3}\left[\frac{E_c + \overline{E_3}}{\underline{R_2}} + I_2\right]$$

where $$I_2 = \frac{\overline{E_3}}{R_b}.$$

With the resistance and voltage tolerances, these relations become

$$G_{nc2} = -(1+\sigma)E_3$$
$$= -(1-\sigma)E_2 + (1+\rho)R_3\left[\frac{E_c + (1+\sigma)E_3}{(1-\rho)R_2} + I_2\right] \qquad (2)$$

where $$I_2 = \frac{(1+\sigma)E_3}{R_b}.$$

Algebraic manipulation of equations (1) and (2) will yield

$$R_2 = \frac{\dfrac{[(1-\sigma)E_2 - (1+\sigma)E_3](1-\rho)E_{nc}}{(1+\sigma)(1+\rho)^2 E_2} - \dfrac{E_c + (1+\sigma)E_3}{(1-\rho)}}{I_2 + \dfrac{[(1-\sigma)E_2 - (1+\sigma)E_3](1-\rho)}{(1+\sigma)(1+\rho)E_2} I_1}. \qquad (3)$$

For a positive value of R_2, equation (3) is a monotonically increasing function of E_2 and is substantially independent of E_2 and E_3 if E_2 is much greater than E_3. A reasonable range for E_2 is

$$8E_3 < E_2 < 10E_3 \qquad (4)$$

To maintain a high input impedance, it is desirable to evaluate the effect of the diodes D_1 and D_2. In equation (3), since the coefficient of I_1 is smaller than that of I_2, consequently, diode D_2 should be eliminated if either of these diodes can be dispensed with. In addition, from the definition of I_1 and I_2, it is apparent that R_2 is proportional to R_b. Therefore, the higher the minimum design value of diode back resistance, the higher will be the value of R_2.

Substitution of known values for E_3, R_b, and E_2 reduces equation (3) to the form:

$$R_2 = aE_{nc} - bE_c + c. \qquad (5)$$

In addition, if we assume that E_{nc} is known, values of which will be discussed later, the above equation becomes

$$R_2 = d - bE_c \qquad (6)$$

where

$$b = \frac{1}{(1-\rho)\left[I_2 + \dfrac{[(1-\sigma)E_2 - (1+\sigma)E_3](1-\rho)I_1}{(1+\sigma)(1+\rho)E_2}\right]}$$

$$d = \frac{\dfrac{[(1-\sigma)E_2 - (1+\sigma)E_3](1-\rho)E_{nc}}{(1+\sigma)(1+\rho)^2 E_2} - \dfrac{(1+\sigma)E_3}{(1-\rho)}}{\left[I_2 + \dfrac{[(1-\sigma)E_2 - (1+\sigma)E_3](1-\rho)I_1}{(1+\sigma)(1+\rho)E_2}\right]}$$

Now let us examine the plate circuit.

C. Plate Circuit

In Fig. 3, when tube 1 is nonconducting, I_3 is equal to I_4 and the grid voltage of tube 2 must be at least as positive as ground level. The effect of any grid current that may flow is only to clamp the grid to ground. The conditions that tend to depress the grid voltage of tube 2 to its lowest level are $(E_1)_{min}$, $(R_2)_{max}$, $(R_1)_{max}$. The grid voltage is known to be either at ground potential or at bias level, $-E_3$, therefore the diode currents do not enter into the equations. It is assumed that the leakage plate current is negligibly small compared to the other

etwork currents and can be neglected for design purposes. As a result,

$$\frac{(1-\sigma)E_1 - E_{nc}}{R_1} = \frac{E_{nc}}{R_2}. \tag{7}$$

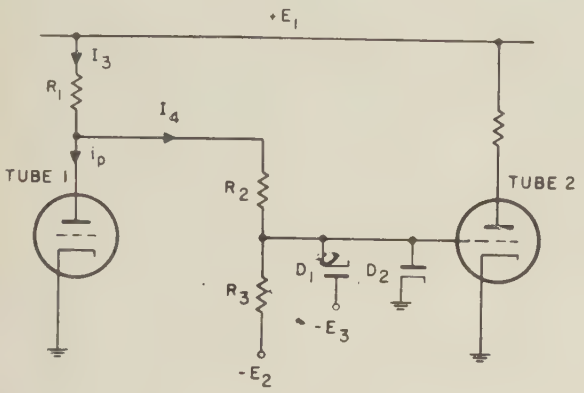

Fig. 3 — Plate circuit.

When tube 1 is conducting, the grid voltage of tube 2 must be at least as negative as the bias level, $-E_3$. The conditions that tend to raise the grid voltage of tube 2 to its highest level are $(E_1)_{max}$, $(R_1)_{min}$, $(R_2)_{min}$, and $(r_p)_{max}$. Therefore,

$$\frac{(1+\sigma)E_1 - E_c}{(1-\rho)R_2} = i_p + \frac{E_c + (1+\sigma)E_3}{(1-\rho)R_2}. \tag{8}$$

From equations (7) and (8)

$$R_2 = \frac{1}{i_p}\left\{\frac{[(1+\sigma)E_1 - E_c]E_{nc}}{(1-\rho)[(1-\sigma)E_1 - E_{nc}]} - \frac{E_c + (1+\sigma)E_3}{1-\rho}\right\}. \tag{9}$$

The values for E_{nc} and E_3 are the same as used in equation (6). In addition, some value is chosen for E_1 that satisfies

$$(1-\sigma)E_1 > E_{nc}.$$

The choice of E_1 is discussed in Section VII. With the substitution of these values, equation (9) becomes

$$R_2 = \frac{1}{i_p}(e - fE_c) \tag{10}$$

where

$$e = \frac{(1+\sigma)E_{nc}E_1}{(1-\rho)[(1-\sigma)E_1 - E_{nc}]} - \frac{(1+\sigma)E}{1-\rho}$$

$$f = \frac{(1-\sigma)E_1}{(1-\rho)[(1-\sigma)E_1 - E_{nc}]}.$$

Further, since the conducting plate voltage $E_c = i_p r_p$

where r_p = maximum permissible static plate resistance,
i_p = plate current

then $$R_2 = \left(\frac{e}{E_c} - f\right)r_p. \tag{11}$$

D. The Complete Solution

An analytical solution of equations (6) and (11) will result in equation (12).

$$r_p = \frac{d - R_2}{\left[\frac{be - fd}{fR_2} + 1\right]f} \tag{12}$$

Appendix I proves that in practical circuits with voltage and component tolerances, $[\ be > fd\ ]$. Therefore, the behavior of equation (12) will be as shown in Fig. 4. Since R_2 also specifies R_s through equation (1)

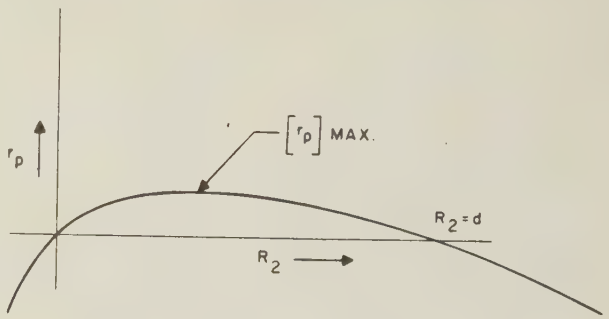

Fig. 4 — r_p as a function of R_2.

(shown in more convenient form as equation (13)), and since R_2 and R_3 determine the dc input impedance of the circuit, equation (12) actually relates the tube plate resistance to the dc input impedance of the circuit.

$$R_3 = \frac{(1+\sigma)E_2}{(1-\rho)\left[\frac{E_{nc}}{(1+\rho)R_2} - I_1\right]} \tag{13}$$

By differentiating equation (12), it can be shown that the maximum r_p in Fig. 4 is:

$$[r_p]_{max} = \frac{2be - df - 2\sqrt{b^2e^2 - bdef}}{f^2}. \tag{14}$$

The corresponding E_c is

$$E_c = \frac{f[r_p]_{max} + d}{2b}. \tag{15}$$

The corresponding R_2 is

$$R_2 = \frac{d - f[r_p]_{max}}{2}. \tag{16}$$

A more convenient form of equation (14) for computational purposes can be derived by a Taylor series approximation. This is given in equation (17).

$$[r_p]_{max} = \frac{d^2}{4be}\left[1 + \frac{1}{2}\left(\frac{df}{be}\right) + \frac{5}{16}\left(\frac{df}{be}\right)^2\right] \tag{17}$$

The error of this approximation is the remainder of the series within the brackets and is less than

$$\frac{7}{32}\left(\frac{\frac{df}{be}}{1 - \frac{df}{be}}\right)^3 \cdots$$

A comparable form for R' is Equation (18).

$$R_2 = \frac{d}{2}\left\{1 - \frac{df}{4be}\left[1 + \frac{1}{2}\left(\frac{df}{be}\right) + \frac{5}{16}\left(\frac{df}{be}\right)^2\right]\right\} \tag{18}$$

Together with other equations already given, equations (14) through (18) complete the solution of the circuit of Fig. 1. R_1 is computed from equation (7), while R_3 is computed from equation (13).

In the solution above, a known value of E_{nc} has been assumed, from which a value for E_1 can be deduced. The following section shows the behavior of the solution as a function of E_{nc} and leads to an optimum value of E_{nc} based on the requirements imposed on the circuit of Fig. 1.

It may be observed that as r_p increases, R_1 also increases. A circuit that permits the maximum r_p will therefore result in the minimum power consumption for any given supply voltage, E_1.

E. Optimizing the Solution for Three Circuit Requirements

It is shown in Appendix II that equation (17) can be maximized with respect to E_{nc}. (Maximization with respect to E_{nc} can best be done by calculating r_p for various values of E_{nc} since a simple expression does not appear to be available for the maximum condition.) Fig. shows the behaviour of $r_{p_{max}}$ and R_2 as functions of E_{n} It is evident that maximization of r_p with respect to E results in a smaller value of R_2 — and consequently, dc input impedance — than could otherwise be attaine A similar conclusion can be reached from Fig. 4 whi shows that the maximum r_p with E_{nc} fixed is not a companied by the maximum R_2. As a result, where dc i put impedance is of paramount importance, the maximu r_p may not be used. However, such departure is alwa made at the expense of designing for shorter tube lif

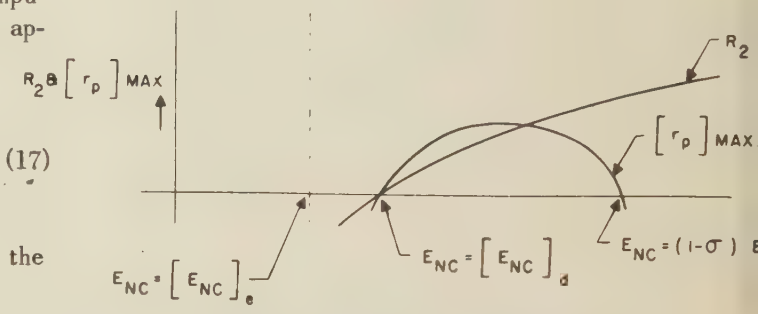

Fig. 5 — R_2 and $[r_p]_{max}$ as functions of E_{nc}.

The design r_p can further be increased by prop choice of E_1. The more nearly the plate load approximat a constant current source, the less current variation needed to obtain a desired plate swing. Alternately, th means that r_p can have a higher value. Both R_1 and can be increased as seen by equation (7) to more near realize such a constant current source. As a result, t design r_p will increase. However, R_1 and E_1 cannot be i creased indefinitely. In order to achieve a desired swit ing time, a certain minimum current must be available the load resistor to drive the capacitance of the attach grid divider. However, as a better approximation to a co stand-current source is realized at the plate load resist the current available for switching decreases. Therefor the choice of R_1 and E_1 must be tempered by switchi time considerations. Conversely, to increase the curre available to drive the capacitance of the grid divider, must be decreased. This, in turn, means a large curre change is needed to swing the plate and r_p cannot be large as otherwise. Guides to the choice of componen based on switching time considerations have been di cussed[1,2].

[1] Rubinoff, Morris, "Further data on the design of Eccles-Jord flip-flops," *Elec. Engineering*, vol. 71, p. 905; October, 195

[2] Buys, W. L., "Analysis of scale units," *Nucleonics;* November, 1948.

The minimum diode back resistance that can be umed is one of the most important parameters in the ign of flip-flops using diodes in the grid circuit. In ations (17) and (18) the ratio d/b is independent of whereas d is directly proportional to R_b. Therefore, the maximum plate resistance as well as the dc input edance increase as the minimum diode back resistance eases.

The optimum design that can be obtained is also endent on the requirements imposed on the circuit that listed under "Assumptions" (Section II A). One set equirements may be:

1. Minimum input signal with no other requirements: this case, an absolute maximum r_p with respect to can be obtained by the methods discussed. Once the uit has been solved, the maximum voltage that the te may encounter is computed. This value, $[E_p]_{max}$, ether with the input signal, E_3, defines a tube μ_{cutoff}

$$\mu_{cutoff} = \frac{[E_p]_{max}}{E_3}.$$

plate resistance of the tube must be less than the ximum r_p defined by the design procedure. DC stable ration is obtained over the range of tube plate resist- e variation from its initial minimum, for a new tube, to maximum design value. The longest tube life is there- obtained from the tube whose initial plate resistance the smallest fraction of the design plate resistance.

Another set of requirements may be:

2. Minimum input signal with specified minimum dc ut impedance. In this case, it is only rarely that the edance requirement can be satisfied at the maximum from case (1). Usually, a smaller r_p must be accepted order to fulfill the input impedance requirement. Con- quently, a shorter tube life will necessarily result. By ying E_{nc} as a design parameter, as in case (1) a $_{utoff}$ and a r_p that will result in the desired dc input edance can be computed.

Conversely, if some particular tube is under con- leration, a value for μ_{cutoff} is known. Then $[E_p]_{max}$, maximum plate voltage that can be held cutoff by a s voltage of $(-E_3)$ is:

$$[E_p]_{max} = E_3 \times \mu_{cutoff}.$$

so, approximately,

$$E_{nc} = (1 - \rho)^2 [E_p]_{max}. \quad (19)$$

is follows from the fact that the cutoff plate voltage both increases and decreases from nominal value as resistor tolerances vay. One configuration of resistor tolerances, together with maximum E_1, results in the maximum plate voltage while another configuration with minimum E_1 results in E_{nc}. Equation (19) is an approximate relation between the two. Thus, a direct solution can be made for the corresponding r_p to determine whether or not the particular tube will yield sufficiently long life in the final circuit.

A final set of requirements will be:

3. Minimum input signal and minimum output voltage: For the circuit of Fig. 1, the minimum output voltage is actually the minimum plate swing. This design problem may arise where low current indicator bulbs are used as output devices. For this case, E_{nc} is varied as a parameter and corresponding E_c is computed until a satisfactory plate swing is obtained. These voltage values determine a value of R_2, as is evident from equation (3), which, in turn, determines a value of r_p. In general, for large plate swings, R_2 is large and, consequently, r_p is decreased; that is, large plate swings serve to decrease the tube life that can be achieved.

Because of the relation in equation (3), the plate swing cannot be specified independently of the dc input impedance. Either an impedance requirement will result in sufficient voltage swing or else a greater voltage swing is required which, in turn, will result in a higher impedance than is required. In either case, one of the requirements is redundant.

Summarizing, it has been shown that the tube plate resistance, r_p, can be maximized with respect to (a) fixed supply voltages, E_1, E_2, and E_3; (b) minimum diode back resistance, R_b; (c) voltage and component tolerances; (d) the design parameter E_{nc}; and (e) the initial requirements imposed on the circuit.

III. SELF-BIASED FLIP-FLOP

Fig. 6 shows a self-biased flip-flop which is often used because of the need for only one power supply and because of the stabilizing effect on voltage swings by the cathode resistor. The diodes D_2 are used to speed-up switching of the circuit by limiting the grid swing and will also permit the insertion of positive trigger pulses. Diodes D_1 permit insertion of negative trigger pulses. Usually, capacitive coupling is used to insert the trigger signals.

The design of the self-biased flip-flop will be achieved in two steps: first, a design will be obtained for the "worst case" of the circuit of Fig. 6 with the modification that the cathode level is assumed to be established by a power supply; second, a proper cathode resistor will be inserted to yield the actual desired circuit.

With respect to resistor tolerances, the "worst case" of reliability for the self-biased flip-flop arises for the minimum cathode voltage, $(E_k)_{min}$. For this condition, the cathode of the nonconducting tube is at its

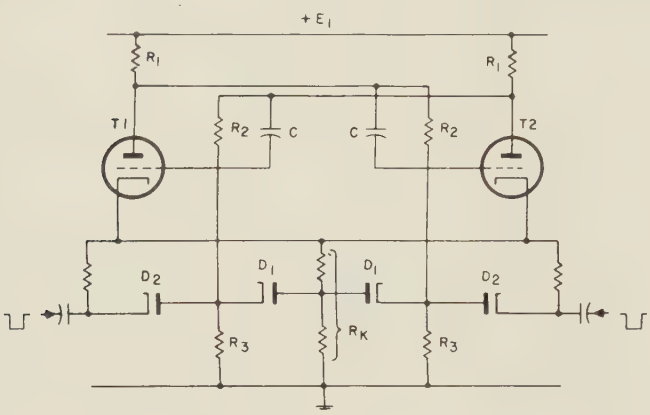

Fig. 6 – Self-biased flip-flop.

least positive level while its grid is at its most positive level. Consequently, the nonconducting tube experiences its least bias; this is the least reliable condition for the nonconducting tube. The minimum cathode voltage $(E_k)_{min}$ is established through cathode follower action by the conducting tube T_1 to correspond to its minimum grid voltage. The minimum grid voltage, however, means the minimum plate current in T_1 so that point A is at its most positive level. The plate current is further minimized by the maximum plate resistance so that $(r_p)_{max}$ is assumed. In addition, the resistor tolerances that cause the grid of the nonconducting tube R_2 to be at its most positive level are $(R_1)_{min}$, $(R_2)_{min}$ and $(R_3)_{min}$. The preceding resistance tolerances together with the effects of the diodes D_1 and D_2 are exactly the same as have been demonstrated for equations (3) and (9).

In Appendix III, the self-biased flip-flop is shown to be independent of variations in the supply voltage, E_1, provided that no diodes are used in the grid dividers. The same condition is very nearly true even when diodes are present so that the tolerance to be used on E_1 is immaterial. For convenience, E_1 will be assumed to be at its nominal value.

A reasonable first approximation to E_2 can also be developed. For efficient use of the grid divider, E_k should be related to the grid swing, E_3, by

$$8\,E_3 < E_k < 10E_3\,.$$

In addition, for a large class of designs, it appears that the nonconducting plate voltage is about 80% of the cathode-to-plate supply voltage. Therefore,

$$(E_p)_{nc} \cong \mu_{co} E_3 \cong 0.8\,(E_1 - E_k)$$

then, using $E_k = 10\,E_o$

$$\frac{\mu_{co}}{10} E_k \cong 0.8\,(E_1 - E_k) \qquad (2$$

or,

$$E_1 \cong E_k\left(1 + \frac{\mu_{co}}{8}\right)$$

With equation (20) as a guide, a first value for E_k chosen.

E_k is next taken as the reference voltage so th the circuit of Fig. 7 is obtained. For this circuit, t design equations for the General Case apply directly wi the sole modification that all the voltage tolerances a zero. Thus, R_1, R_2, R_3 and $(r_p)_{max}$ can be obtained direct

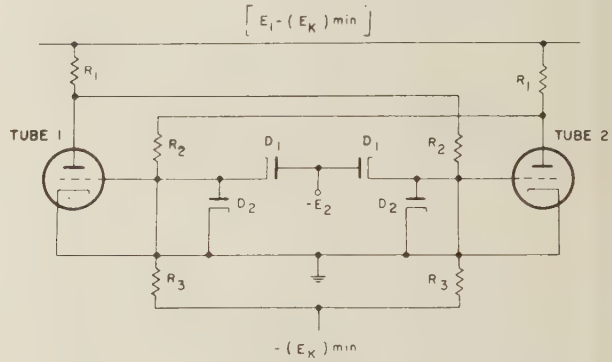

Fig. 7 – Reduced self-biased flip-flop.

It would appear that R_k could next be compute directly since $(E_k)_{min}$ and $(i_p)_{min}$ are known. Howeve variation of R_k within its tolerance limits will modify t permissible degree of tube aging from the previously co puted "worst" tube. Say, for example that the nomin value of R_k is computed from

$$R_k = \frac{(E_k)_{min}}{(i_p)_{min}}\,. \qquad (2$$

If R_k should then decrease within its negative toleranc a smaller cathode-to-grid voltage must result at the co ducting tube and a slightly larger plate current must flo through it. This means that the conducting tube wi reach the condition of zero bias in a shorter time than f the nominal value of R_k. If positive grid operation precluded for design purposes, the tube life is therefo shortened over that obtainable for the nominal R_k. On t other hand, if R_k should increase within its positi tolerance, the conducting tube plate current will decrea This will tend to raise the grid of the nonconducting tu to a higher potential. Consequently, the conducting tu must have a smaller plate resistance in order to hold t nonconducting tube cut off to the specified limits of r liability. Again, the tube life is shortened over that o

tainable for the nominal R_k. Since the magnitude of the two effects can not be evaluated in general, a compromise determination of R_k would appear to be given by equation (21). The greatest degree of permissible aging should then be recomputed for each of the preceding limiting conditions tc determine the "worst case".

If the final circuit does not meet all the imposed conditions, a different value of E_k is chosen and a recomputation made. Finally, a small correction in the values of the two resistors constituting R_k must be made to accommodate the clamping current flowing through diodes D_2. Since all the voltages and currents are known, this presents no difficulty.

IV CONVENTIONAL ECCLES-JORDAN FLIP-FLOP

As another special case, if no clamping diodes are used, or if the clamping diodes have infinite back resistance (vacuum tube diodes), the circuit of Fig. 1 reduces to the conventional Eccles-Jordan circuit shown in Fig. 8.

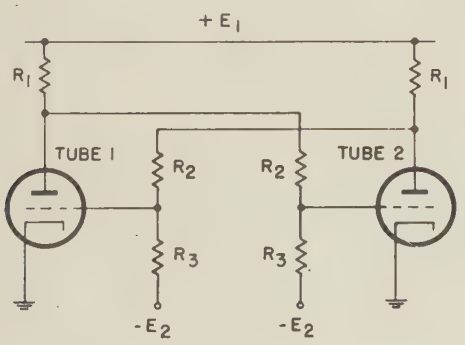

Fig. 8 – Special case.

For this circuit, the diode back currents are zero. Equation (3) therefore takes the form

$$\frac{[(1-\sigma)E_2 - (1+\sigma)E_3](1-\rho)E_{nc}}{(1+\sigma)(1+\rho)^2 E_2} = \frac{E_c + (1+\sigma)E_3}{(1-\rho)}. \quad (22)$$

Solving equation (22) for E_c,

$$E_c = K E_{nc} - (1+\sigma) E_3 \quad (23)$$

$$K = \frac{(1-\rho)^2 [(1-\sigma)E_2 - (1+\sigma)E_3]}{(1+\sigma)(1+\rho)^2 E_2}.$$

Eliminating E_c from equations (11) and (23) will result in equation (24).

$$r_p = \frac{R_2}{\frac{e}{K E_{nc} - (1+\sigma) E_3} - f}. \quad (24)$$

It can be shown that r_p, as a function of E_{nc}, behaves as shown in Fig. 9. Consequently, r_p for the circuit of Fig. 8 can be maximized with respect to E_{nc} for a set of given values for E_1, E_2, and E_3. An actual value of r_p can only be specified if a value is specified for R_2. If a dc input impedance figure is not specified, then switching time requirements will serve as the limiting value for R_2. Once R_2 is specified, r_p is determined and the remaining components, R_1 and R_3, are found from equations (7) and (13), respectively.

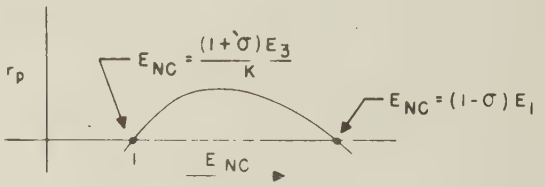

Fig. 9 – r_p as a function of E_{nc}.

V. GENERAL CASE WITH OUTPUT DIVIDER

In order to derive a usuable output signal from a flip-flop, an output divider may be added as in Fig. 10.

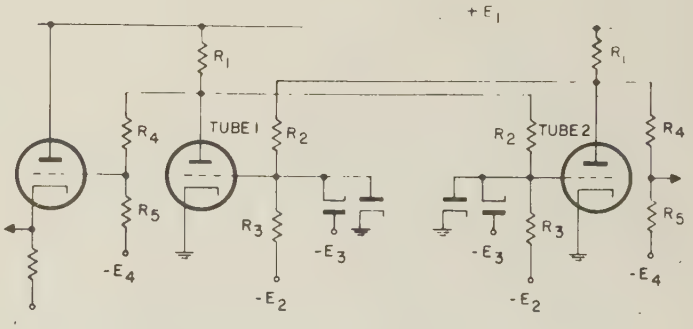

Fig. 10 – General case with output divider.

The effect of the presence of the output divider is to reduce the maximum plate resistance that can be tolerated in the circuit. In order to provide current to the nonconducting case, the load resistance, R_1, must be reduced. In order, therefore, to cause a sufficient fall in the plate voltage for the conduction case, the maximum plate resistance must be smaller in order to compensate for the smaller load resistance. Thus, the use of an output divider will decreaşe the design tube life for the circuit.

To obtain an analytic design for this configuration, an output divider of a fixed impedance is assumed. E_{nc} is assumed known so that a current value due to the output divider can be added into equation (7) to obtain

$$\frac{(1-\sigma)E_1 - E_{nc}}{(1+\rho)R_1} = \frac{E_{nc}}{(1+\rho)R_2} + I_5 \qquad (25)$$

$$I_5 = \frac{E_{nc} + (1+\sigma)E_4}{(1-\rho)(R_4+R_5)}.$$

When tube 1 conducts, the current term due to the output divider may be added to equation (8) to obtain

$$\frac{(1+\sigma)E_1 - E_c}{(1-\rho)R_1} = i_p \frac{E_c + (1+\sigma)E_3}{(1-\rho)R_2} + \frac{E_c + (1-\sigma)E_4}{(1+\rho)(R_4+R_5)}. \qquad (26)$$

Equations (25) and (26) can be solved to obtain

$$R_2 = \frac{\dfrac{[(1+\sigma)E_1 - E_c]E_{nc}}{(1-\rho)[(1-\sigma)E_1 - E_{nc}]} - \dfrac{E_c + (1+\sigma)E_3}{1-\rho}}{i_p - \dfrac{I_5(1+\rho)[(1+\sigma)E_1 - E_c]}{(1-\rho)[(1-\sigma)E_1 - E_{nc}]} + \dfrac{E_c + (1-\sigma)E_4}{(1+\rho)(R_4+R_5)}}. \qquad (27)$$

Referring to equation (11), equation (27) can be put into a similar form so that

$$R_2 = \frac{e - fE_c}{ip + hE_c - g} \qquad (28)$$

$$g = \frac{I_5(1+\rho)(1+\sigma)E_1}{(1-\rho)[(1-\sigma)E_1 - E_{nc}]} - \frac{(1-\sigma)E_4}{(1+\rho)(R_4+R_5)}$$

$$h = \frac{(1+\rho)I_5}{(1-\rho)[(1-\sigma)E_1 - E_{nc}]} + \frac{1}{(1+\rho)(R_4+R_5)}$$

Proceeding to solve equations (28) and (6) in the same manner as before

$$r_p = \frac{d - R_2}{f\left[1 + \dfrac{be - df}{fR_2} + \dfrac{bg - h(d - R_2)}{f}\right]}. \qquad (29)$$

The maximum r_p is obtained for a value of R_2 such that

$$R_2 = \frac{df - be}{bg + f}\left[1 - \sqrt{1 - \frac{d(bg+f)}{df - be}}\right]. \qquad (30)$$

Corresponding to this, the maximum r_p becomes

$$[r_p]_{max} = \frac{1}{\dfrac{be - df}{R_2^2} - h} \qquad (31)$$

while

$$E_c = \frac{d - R_2}{b}. \qquad (32)$$

Calculations can then be made for other values of E_{nc} to determine whether a more favorable configuration can be achieved. R_1 and R_3 are found from equations (25) and (13), respectively.

After the circuit is solved so that both E_{nc} and E_c are known, the minimum output swing available at the cathode follower grid can be determined. The dc level is adjusted by proportioning R_4 and R_5. The output swing can be increased by increasing E_4 and R_5 in equation (23) in such a manner as to maintain I_5 a constant. Such a change has a second order effect on equation (26) and will not, therefore, appreciably affect the total solution. Since the output swing is limited to some fraction of $(E_{nc} - E_c)$, it may be necessary to increase the plate swing in some cases. A satisfactory solution is found by increasing E_{nc} and repeating the calculations. As discussed previously, the larger plate swing will, in most cases, result in a shorter tube life.

VI NUMERICAL EXAMPLE

A. Assumptions

Circuit Specifications:

1. Input signal = 15 volts, therefore: $-E_3 = -15$ volts
2. DC drain into input less than 0.75 milliamperes
3. Output divider swing to cathode follower: 0 to -25 volts
4. Resistor tolerances = ± 8%
5. Voltage tolerances = ± 5%
6. Diode back resistance = 80,000 ohms
7. Diode D_2 not desired [therefore: $I_2 = 0$]
8. Given supply voltages: E_1 = 250 volts, $-E_2$ = -200 volts, $-E_4$ = -200 volts
9. Output divider impedance $(R_4 + R_5)$ in the range 600,000 to 700,000 ohms: try 660,000 ohms

Assume: E_{nc} = 180 volts.

B. Computed Values

Solutions: To find	Use Equation
b, d	(6)
e, f	(10)
g, h	(28)
$r_{p\,max}$	(31)

R_2	(30)
R_1	(25)
R_3	(13)
R_4, R_5	Cut-and-try from values of E_{nc} and E_c

Substituting as indicated,

b	$= 7.70 \times 10^3$
d	$= 7.08 \times 10^5$
e	$= 870$
f	$= 4.46$
g	$= 3.14 \times 10^{-3}$
h	$= 14.0 \times 10^{-6}$
$r_{p\ max}$	= 12,900 ohms
R_2	= 197,000 ohms
R_1	= 36,000 ohms
R_3	= 354,000 ohms
R_4	= 270,000 ohms } Yield output swing from
R_5	= 390,000 ohms } 1 volt to -27 volt

Also, it can be found that

$$[E_p]_{max} = 211 \text{ volts}$$

$$\text{Therefore, } \mu_{cutoff} = \frac{211}{15} = 14$$

A satisfactory tube would be the 12AV7 which satisfies μ_{cutoff} and has a new tube plate resistance of approximately 5,000 ohms. Operation should be realized for decrease of zero bias plate current to 37% of new tube value.

The dc equivalent input circuit for a new 12AV7 tube is a 48,000 ohm resistor returned to -35 volts. Therefore, the total dc input current drain is 0.73 milliamperes.

The final circuit shown in Fig. 11 satisfies all the specifications imposed on the circuit.

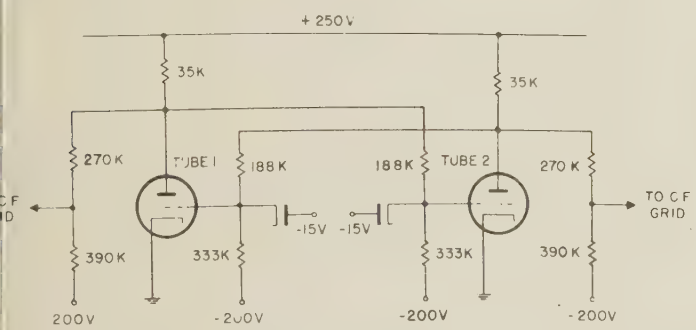

Fig. 11 — Illustrative flip-flop.

Choice of RMA Values

The circuit as shown has the disadvantage of using resistors that are not RMA values. In order to obtain RMA values, it is sufficient, in most cases, to increase the resistor tolerance by 2% and choose resistors differing from the computed value within the resultant 4% range. Such values still satisfy the original resistor tolerances specified.

APPENDIX I

Discussion of the Three Possible Cases of the Solution for R_2

The behavior of equations (6) and (11) as in Fig. 12 shows that the solution is a quadratic with three special cases for the coefficients.

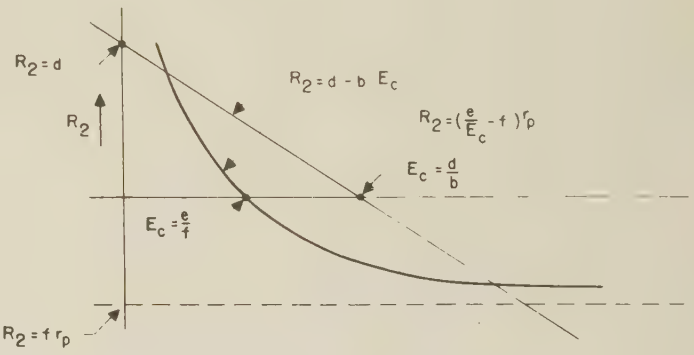

Fig. 12 — Equations for solutions of R_2.

The three special cases for the coefficients are:

$$\text{Case I} \quad \frac{e}{f} < \frac{d}{b}$$

$$\text{Case II} \quad \frac{e}{f} = \frac{d}{b}$$

$$\text{Case III} \quad \frac{e}{f} > \frac{d}{b}$$

It is shown below that Cases I and II are not usually encountered. From Equation (6),

$$\frac{d}{b} = \frac{\dfrac{[(1-\sigma)E_2 - (1+\sigma)E_3]\ (1-\rho)E_{nc}}{(1+\sigma)\ (1+\rho)^2\ E_2} - \dfrac{(1+\sigma)E_3}{(1-\rho)}}{\dfrac{1}{1+\rho}}.$$

For $E_2 >> E_3$, and $E_{nc} >> E_3$

$$\frac{d}{b} = \frac{(1-\sigma)\ (1-\rho)^2}{(1+\sigma)\ (1+\rho)^2} E_{nc}.$$

From equation (10),

$$\frac{e}{f} = \frac{\dfrac{(1+\sigma)E_{nc}E_1}{(1-\rho)[(1-\sigma)E_1 - E_{nc}]} - \dfrac{(1+\sigma)E_3}{1-\rho}}{\dfrac{(1-\sigma)E_1}{(1-\rho)[(1-\sigma)E_1 - E_{nc}]}}.$$

For $E_{nc} >> E_3$

$$\frac{e}{f} = \frac{(1+\sigma)}{(1-\sigma)}E_{nc}.$$

Therefore, for the conditions cited,

$$\frac{e}{f} > \frac{d}{b}$$

since

$$\frac{(1+\sigma)}{(1-\sigma)}E_{nc} > \frac{(1-\sigma)(1-\rho)^2}{(1+\sigma)(1+\rho)^2}E_{nc}$$

or

$$1 > \frac{(1-\sigma)^2(1-\rho)^2}{(1+\sigma)^2(1+\rho)^2}$$

which is always satisfied.

Therefore, in practical solutions where voltage and component tolerances must be considered, only Case III is of significance. Fig. 13 is a replot of Fig. 10 for the conditions imposed by Case III with r_p a variable.

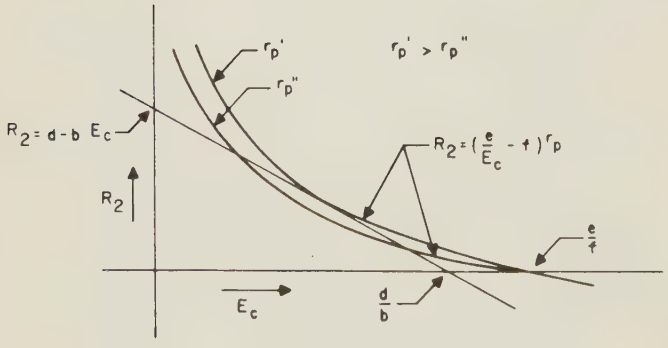

Fig. 13 — Special case for equations of Fig. 12.

As can be seen, the solution in general results in two distinct, real values for R_2. However, the solution can be made to degenerate to one distinct root by considering a sufficiently large value of r_p. This maximum value of r_p actually represents the most aged tube that can be designed for use with the particular voltage configuration and tolerances considered.

APPENDIX II

Behavior of Maximum Tube Plate Resistance With Regard to E_{nc}

It will be shown that $[r_p]_{max}$ as given by equation (17) can also be maximized with respect to E_{nc}. In equation (17), d, e and f are functions of E_{nc}. From an examination of the expressions for d and e, it is observed that both d and e have a zero for some positive E_{nc}. From the expressions for e and f, it is also seen that both e and f have a pole for $E_{nc} = (1-\sigma)E_1$. To show that the zero of d occurs for a higher value of E_{nc} than the zero of e, let $[E_{nc}]_d$ yield the zero of d and $[E_{nc}]_e$ yield the zero of e. Then from $d = 0$,

$$[E_{nc}]_d = \frac{(1+\sigma)^2(1+\rho)^2E_2E_3}{(1-\rho)^2[(1-\sigma)E_2 - (1+\sigma)E_3]}$$

while, from $e = 0$,

$$[E_{nc}]_e = \frac{(1-\sigma)E_1E_3}{E_1 + (1+\sigma)E_3}.$$

To prove that

$$(E_{nc})_d > (E_{nc})_e$$

or, equivalently, that

$$\frac{(1+\sigma)^2(1+\rho)^2E_2E_3}{(1-\rho)^2[(1-\sigma)E_2 - (1+\sigma)E_3]} > \frac{(1-\sigma)E_1E_3}{E_1 + (1+\sigma)E_3}.$$

Let

$$K = \frac{(1-\sigma)(1-\rho)^2}{(1+\sigma)(1-\rho)^2}$$

and observe that $k < 1$. Then

$$E_2[E_1 + (1+\sigma)E_3] > KE_1[(1-\sigma)E_2 - (1+\sigma)E_3]$$

$$E_1 E_2 [1 - K(1-\sigma)] + E_3 [K(1+\sigma) + K(1+\sigma)E_1] > 0$$

where the lefthand member is seen by inspection to be always positive.

As a consequence of $[E_{nc}]_d > [E_{nc}]_e$, the behavior of $[r_p]_{max}$ as a function of E_{nc} is illustrated by the curve in Fig. 5.

APPENDIX III

The Effect of Plate Supply Variations on the Self-Biased Flip-Flop

It will be shown that the self-biased flip-flop is independent of variations in the supply voltage when no diodes are used in the grid divider. For convenience, all resistors indicated in Fig. 14 are assumed to be the "worst case".

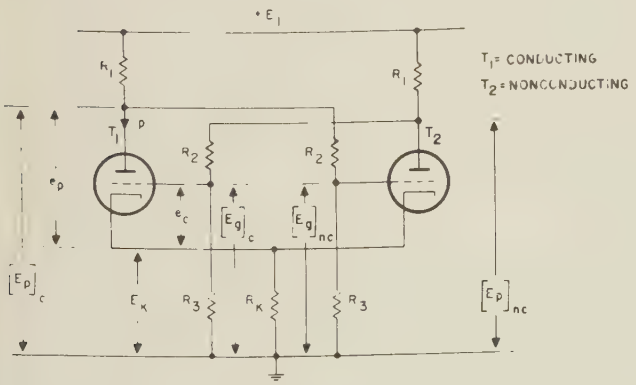

Fig. 14 — Self-biased flip-flop without clamps.

It is evident from Fig. 14 that

$$(E_g)_c = \frac{R_3}{R_1 + R_2 + R_3} E_1 = \alpha E_1$$

$$(E_p)_{nc} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} E_1 = \beta E_1$$

Now, $i_p = \frac{e_p}{r_p} + gm\, e_c$

where, $e_p = E_1 - i_p r_k - R_1 \frac{(i_p + i_p R_K + e_p)}{R_2 + R_3}$

or

$$e_p = \frac{e_1 - i_p \left[R_k + \left(1 + \frac{R_k}{R_2 + R_3}\right) R_1 \right]}{1 + \frac{R_1}{R_2 + R_3}}$$

and

$$e_c = -E_k + (E_g)_c$$
$$= -i_p R_k = \alpha E_1 .$$

From which

$$i_p = \frac{1}{r_p} \left[\frac{E_1 - i_p \left[R_k + R_1 \left(1 + \frac{R_k}{R_2 + R_3} \right) \right]}{1 + \frac{R_1}{R_2 + R_3}} \right]$$
$$+ \frac{\mu}{r_p} (\alpha E_1 - i_p R_k).$$

So that

$$i_p = \frac{E_1 (1 + \alpha \mu)}{r_p + \frac{R_k + R_1 \left(1 + \frac{R_k}{R_2 + R_3} \right) + \mu R_k}{1 + \frac{R_1}{R_2 + R_3}}}$$
$$= \gamma E_1 .$$

Consequently,

$$(E_p)_c = E_k + e_p$$
$$= i_p R_k + (i_p r_p - \mu e_c)$$
$$= i_p (R_k + r_p) - \mu (\alpha E_1 - R_k \gamma - E_1)$$
$$= \gamma E_1 (R_k + r_p) - \mu (\alpha E_1 - R_k \gamma E_1)$$
$$= \lambda E_1$$

while

$$E_k = i_p R_k$$
$$= \epsilon E_1$$

and

$$(E_g)_{nc} = \frac{R_3}{R_2 + R_3}(E_p)_c$$
$$= \theta E_1.$$

Finally the ratio, R, of plate voltage to grid voltage for the nonconducting tube is

$$R = \frac{(E_p)_{nc} - E_k}{E_k - (Eg)_{nc}}$$
$$= \frac{\beta E_1 - \epsilon E_1}{\epsilon E_1 - \theta E_1}$$
$$= \frac{\beta - \epsilon}{\epsilon - \theta}$$

So that the reliability of cutoff of the nonconducting tube is independent of supply voltage variations.

Further, the bias voltage, e_c, of the conducting tube is

$$e_c = -i_p R_k + \alpha E_1$$
$$= (-\lambda R_k + \alpha) E_1 .$$

If the resistor values and the conducting tube plate resistance are such that $\alpha = \lambda \bar{R}_k$, the bias voltage remains zero regardless of variations in E_1. That is, the permissible degree of tube aging is only a function of the resistor values and tube plate resistance and is not affected by variations in E_1.

CONTRIBUTORS

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CORRECTION

The following Tables replace Tables I and II of the paper "Symbolic Programming" by N. Rochester which appeared on pages 10 and 11 of the March 1953 issue of *Transactions* (vol. EC-1, no. 1).

TABLE I
An Actual Program Which Has Been Modified

	LOCATION	±	INSTRUCTIONS OR DATA: OPERATION PART	ADDRESS PART	
	0288	+	STORE	0868	
	0289	+	R ADD	0702	
	0291 ~~0290~~	+	ADD	0750	
	0292 ~~0291~~	+	STORE A	~~0292~~	0293
	0293 ~~0292~~	+	R ADD	(0000)	
	0290	+	A LEFT	0001	

TABLE II
A Symbolic Program Which Has Been Modified

	LOCATION	±	INSTRUCTIONS OR DATA: OPERATION PART	ADDRESS PART	
	11.8	+	STORE	14.9	
	11.9	+	R ADD	13.4	
	11.10	+	ADD	15.8	
	11.11	+	STORE A	11.12	
	11.12	+	R ADD	(0000)	
	11.9.1	+	A LEFT	0001	

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